EPFL Technologies of Nanofabrication

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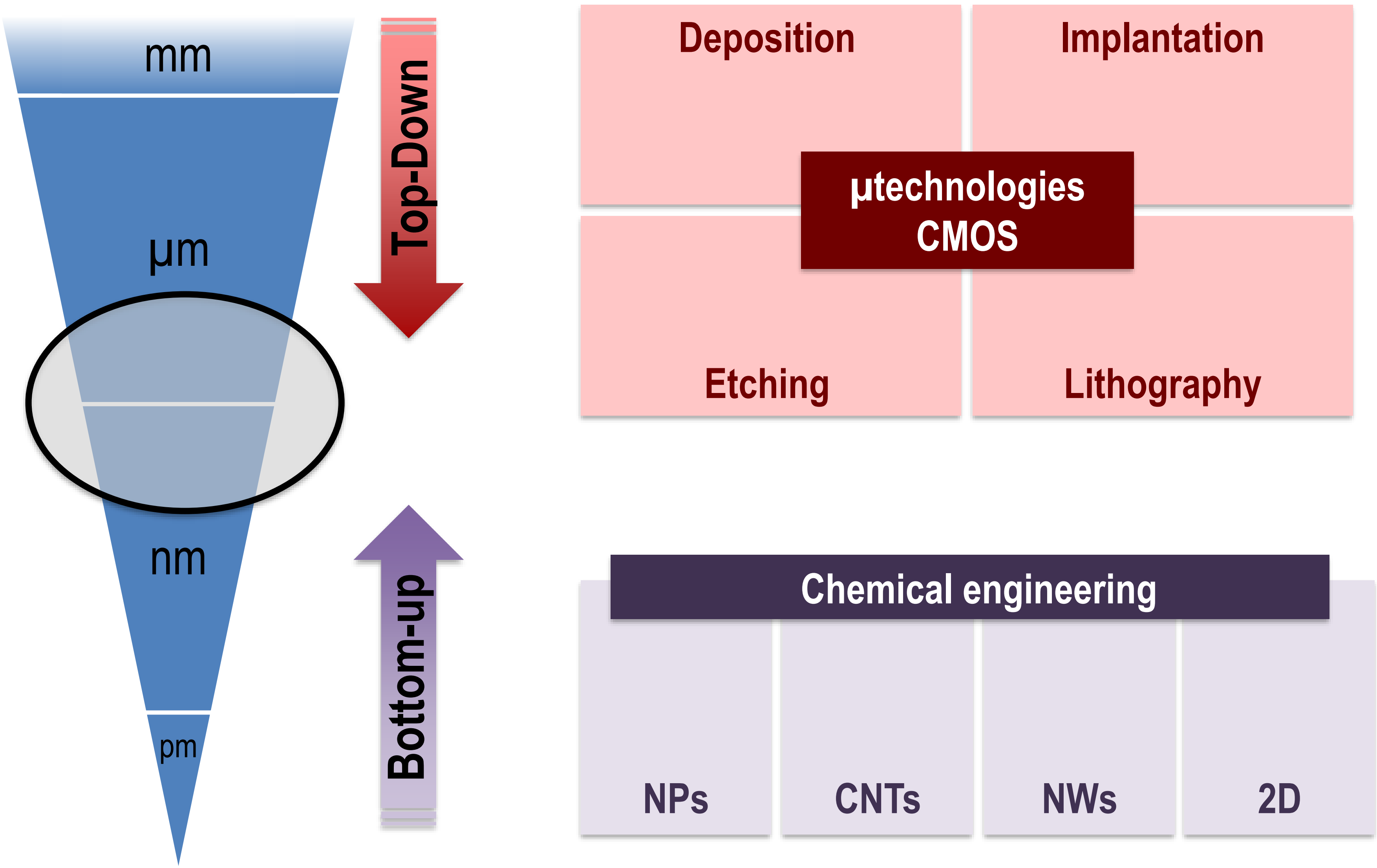
- Ph.D. at IMB-CNM (2006) – Barcelona
- PostDoc at EPFL (2007-2009)
- MC PostDoc at Caltech (2009-2012)
- MC PostDoc at DTU (2012-2013)
- Assistant Professor at EPFL (July 2013 - …)
  - Resonant NEMS&MEMS
  - Pushing the limits of fabrication tools

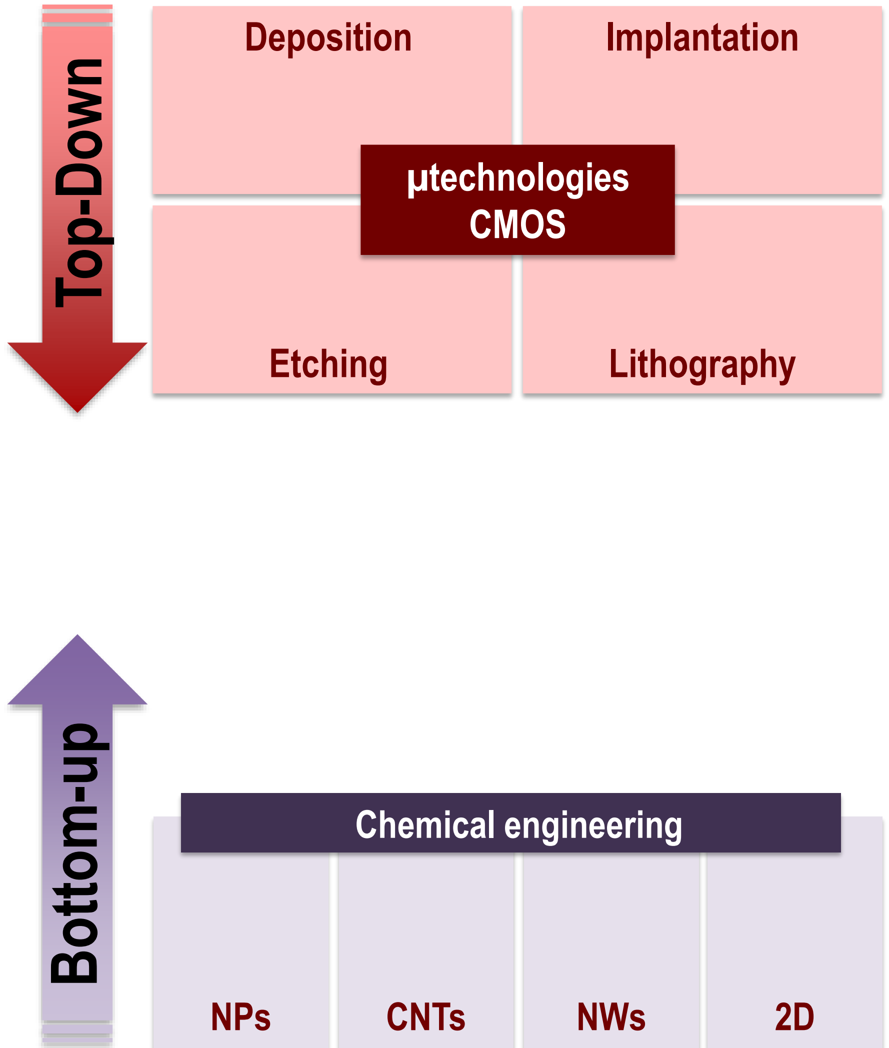
- Static NEMS
- Nanofabrication
- Resonant NEMS

Technologies of Nanofabrication



Technologies of Nanofabrication

- Challenges
  - Many different techniques to cover
  - Diverse backgrounds
    - Some of you might know most of what I am going to talk about
    - Some of you might have never handled a wafer
  - Relation with other courses
  - Main challenge – this is online!!!



EPFL

Top-Down Methods

Deposition

Implantation

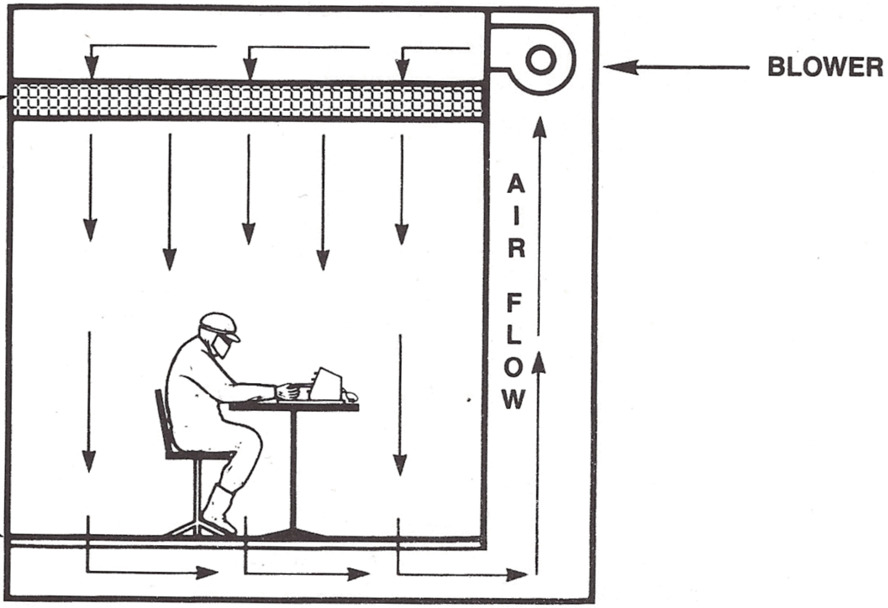
µtechnologies
CMOS

Etching

Lithography

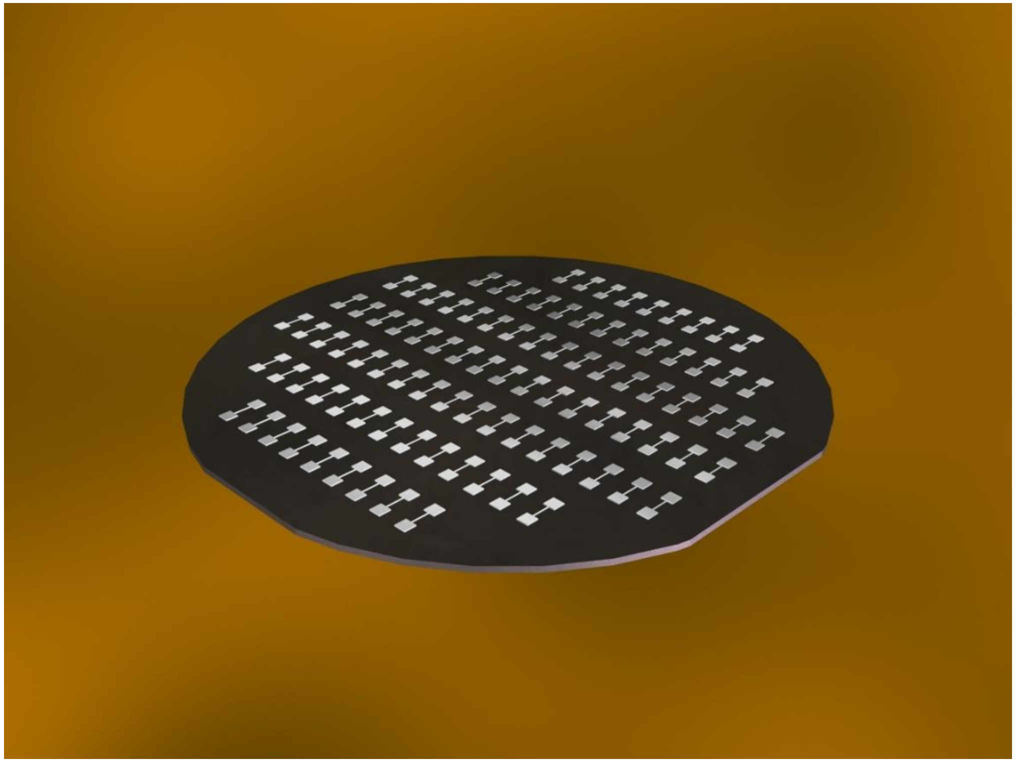
Cleanroom

- Controlled environment to perform the processes
  - Temperature and humidity are kept constant
  - P above 1 atm
  - Air filtered continuously
- Classified as a function of # of particles $\leq 0.5\mu m$ in a *cubic foot*, e.g.
  - Class 100
  - Class 10000
  - Higher class # = worse cleanroom



Planar technology

- Silicon wafers are the main substrate
- Everything is fabricated by adding layers of different materials which are later partially removed
- Most processes affect the whole surface simultaneously



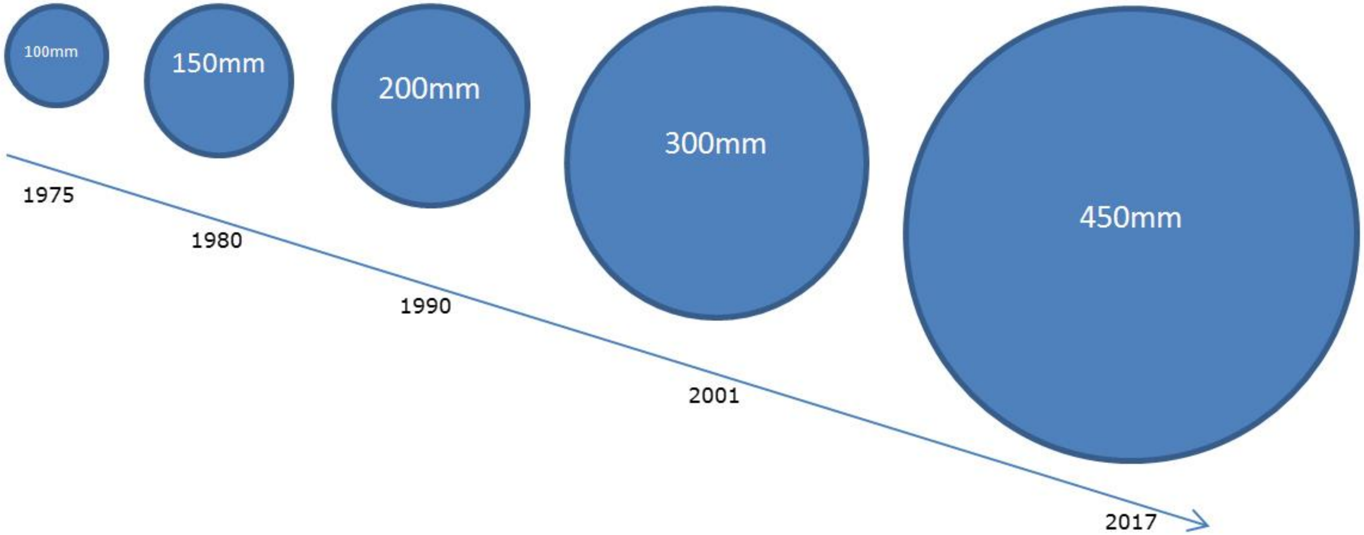
Wafers

- Everything starts with Silicon grains
- The Czochralski method

https://www.youtube.com/watch?v=AMgQ1-HdElM

Wafers

- Everything starts with Silicon grains
- The Czochralski method
- Tendency to increase wafer diameter
  - # of chips per wafer ↗ - $radius^2$
  - # of steps per wafer is constant
    - Uniformity across the wafer is challenging
  - Cost per chip ↘



Lithography (I)

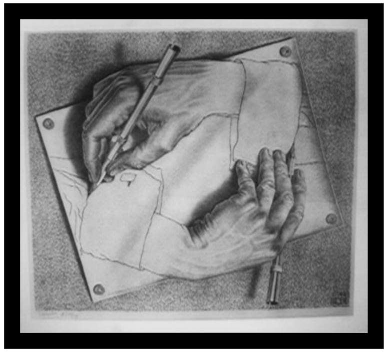
Summary table

Deposition	Implantation
Etching	Lithography

TOP-DOWN

Definition of lithography

- **Lithography** (*lithos* + *graphos*) - method to print on a smooth surface



Drawing

Printing

- In micro/nano fabrication
  - it defines patterns on polymer layers so that they can be transferred to the underlying materials/layers.

https://www.youtube.com/watch?v=1bxf9QRVesQ

Types of lithography

- Optical lithography
- Electron Beam Lithography (EBL)
- Nano Imprint Lithography (NIL)
- Scanning Probe Lithography (SPL)
- Nano Stencil Lithography (nSL)
- Directed Self Assembly Lithography (DSAL)
- …

- Why is lithography so important?
  - It establishes the first limitation to the minimum features that can be transferred

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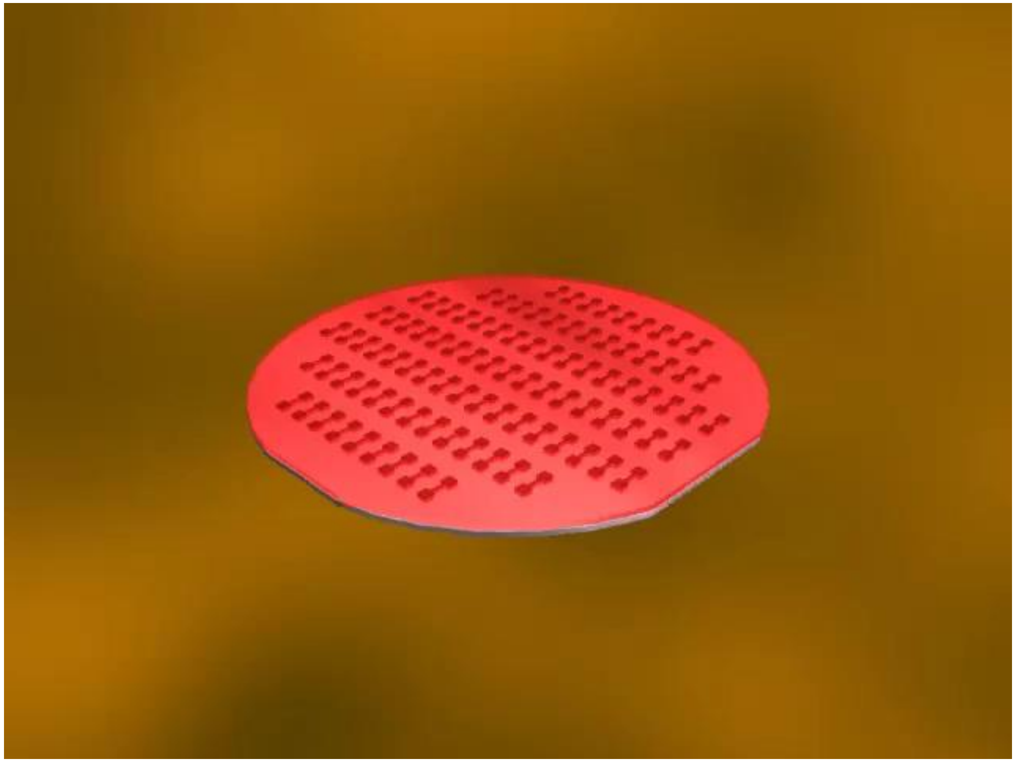
Steps

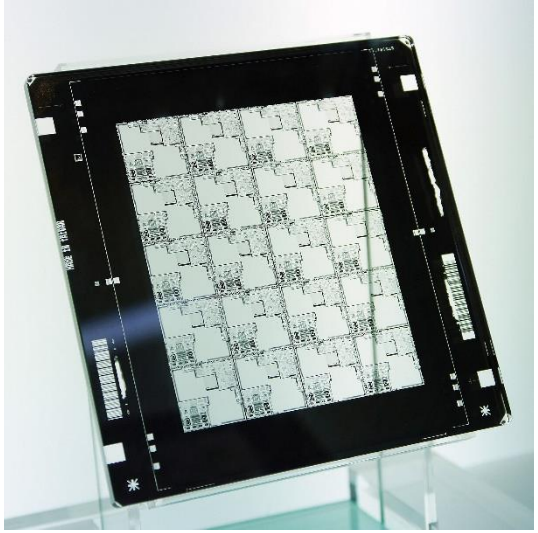
- Preparation of design and mask
- Coating
- Exposure
- Development

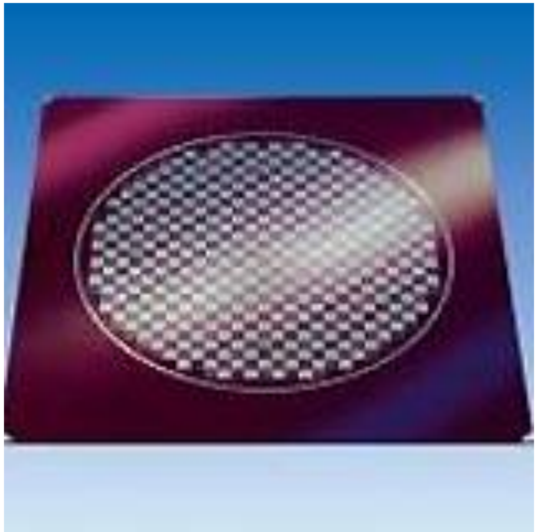


Mask fabrication

- A mask is a glass/quartz plate with chromium (or other opaque material) on top
- Cr is removed from some places according to the design so that light can pass through and illuminate some zones of the wafer

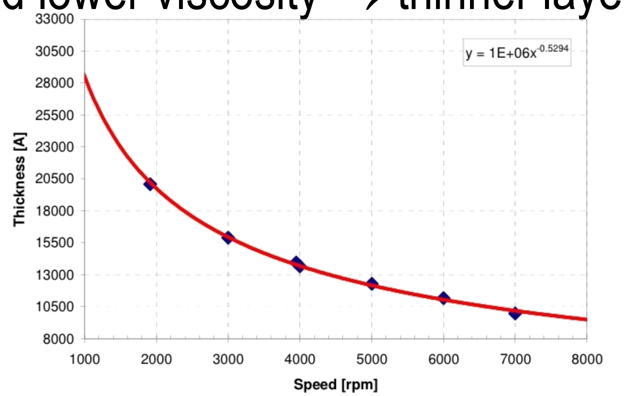
- Masks are written with Electron Beam Lithography or Direct Laser Writing

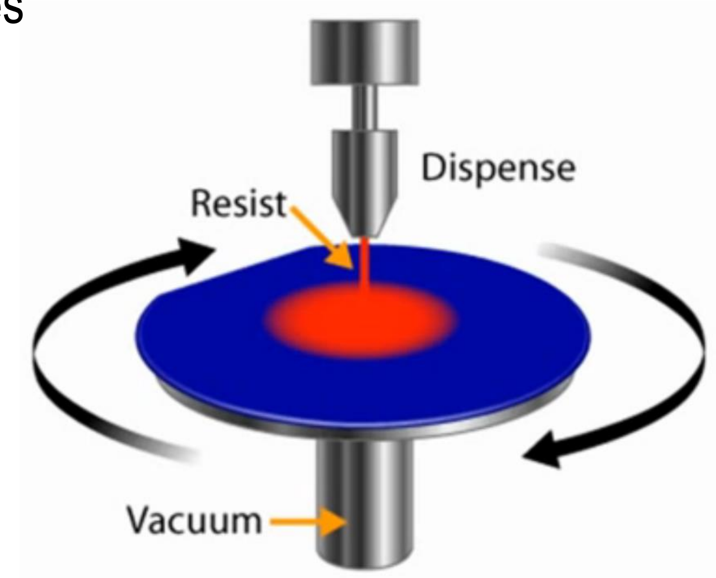




Coating

- Surface conditioning
  - Preparation of the wafer surface to improve resist adhesion
  - Dehydration + HMDS (HexaMethylDiSilazane) – Hydrophobic surface
- Resist deposition
  - Critical step as it determines thickness and uniformity
  - Spin Coating: resist is dispensed on top and wafer spins at a certain speed
  - Balance between centrifugal force and viscous forces
  - Higher speed and lower viscosity → thinner layer



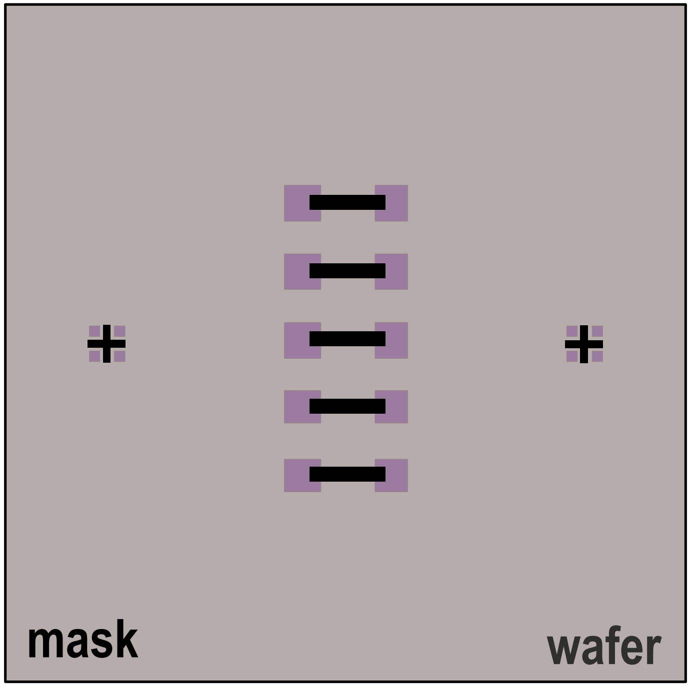


- Soft bake
  - Step to remove solvent from resist
  - Solidifies the resist

Exposure

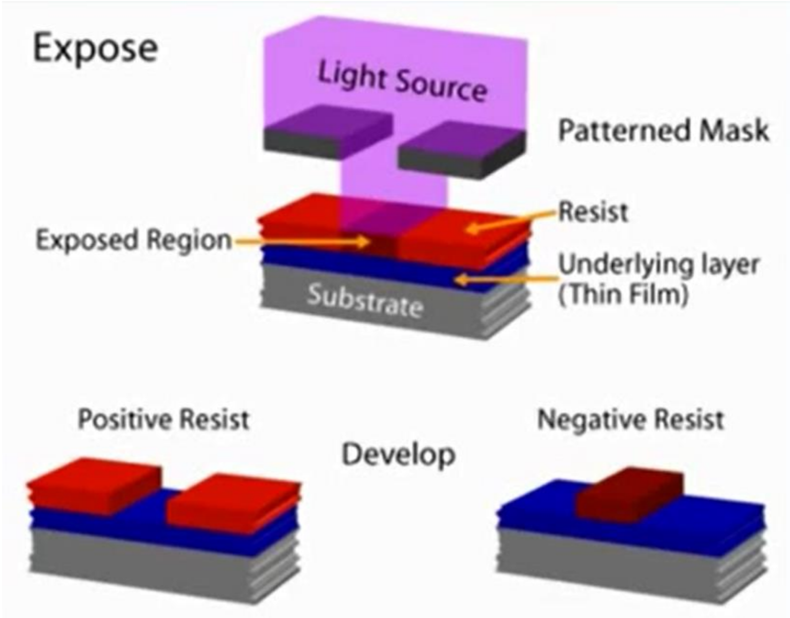
- Alignment
  - Critical process to fabricate multi-layered structures/systems
  - Manual – precision of 1 μm
  - Automatic – pattern recognition software – <100 nm

- Exposure
  - Where the mask does not have Cr



Resist

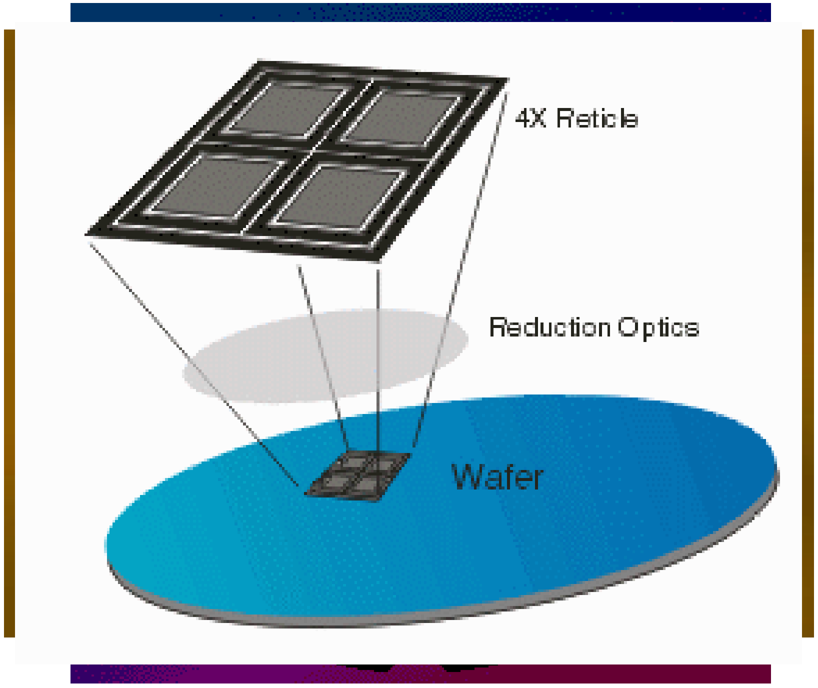
- Resists are radiation sensitive polymers
- Negative resist
  - Cross-linking: adjacent chains cross-connect to increase molecular weights
  - Exposed zone remains
- Positive resist
  - Chain-scission: reduction of average molecular weight.
  - Exposed zone is removed



Exposure

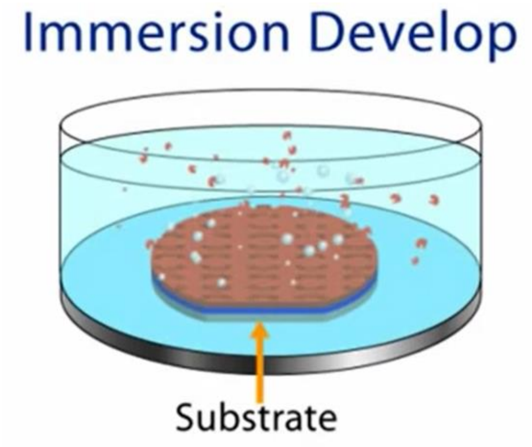
- Alignment
  - Critical process to fabricate multi-layered structures/systems
  - Manual – precision of 1 µm
  - Automatic – pattern recognition software – <100 nm

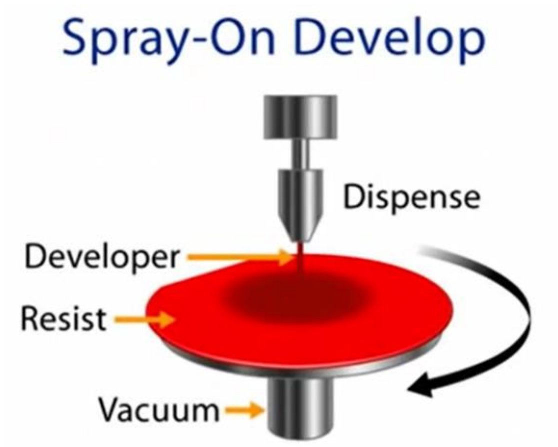
- Exposure
  - Where the mask does not have Cr
  - Can be done on full-wafer (mask)
    - Contact
    - Proximity
  - Or in “steps”, using a reticle and a stepper
    - Projection
  - Exposure time depends on
    - Resist – Type and Thickness
    - Substrate
    - Lamp – Wavelength and Power



Development

- Development
  - Wafer is put in contact with a chemical (developer) that selectively removes exposed/unexposed parts of the wafer





- Hard-Bake
  - Hardening of resist
  - Increase selectivity for etching

Main issues Litho

-
-
-
-
-
-
-

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Lithography (II)

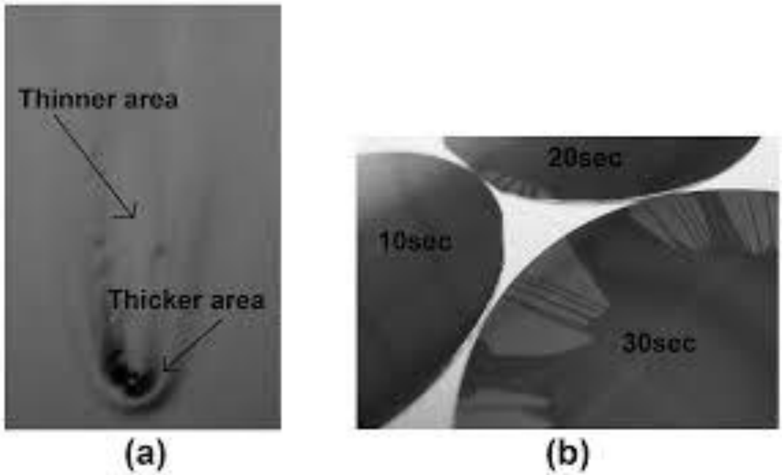
Main issues

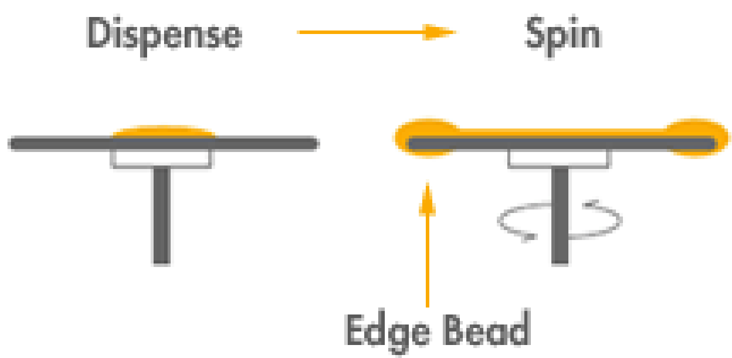
- **Coating**
  - Adhesion of resist to underlying material
  - Non-uniform coating
  - Edge Bead Removal
- **Bake (pre/post/hard)**
  - Reflow
  - Sticking to mask
  - Resist stripping
  - Etch selectivity
- **Exposure**
  - Reflectance of substrate
  - Wavelength of light
  - Hydration of resist
- **Development**
  - Substrate damage

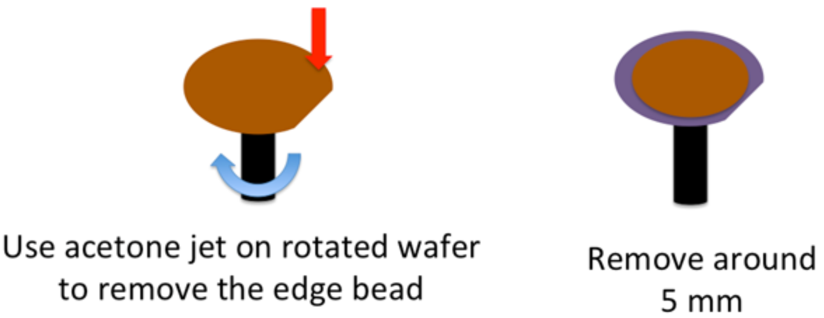
http://www.microchemicals.com/technical_information/TroubleShooter_EN.pdf

Main issues

- Coating
  - Adhesion of resist to underlying material
    - Proper dehydration, HMDS…
  - Non-uniform coating
    - Dispensing more
    - Avoid bubbles and particles
    - Avoid too long between casting and spinning
  - Edge Bead Removal



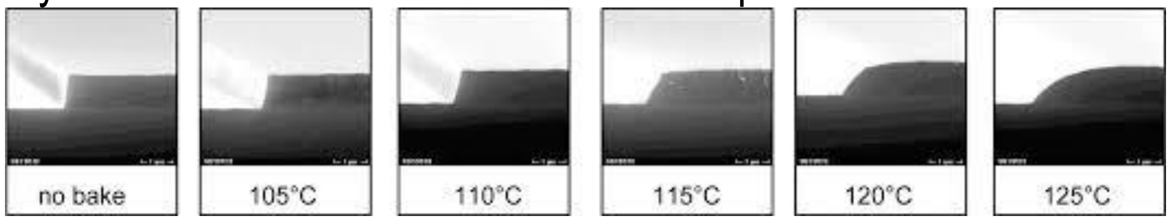




http://www.microchemicals.com/technical_information/TroubleShooter_EN.pdf

Main issues

- Bake (pre/post/hard)
  - Sticking to mask
    - Probably solvent excess still in the resist → Proper soft-bake
  - Reflow

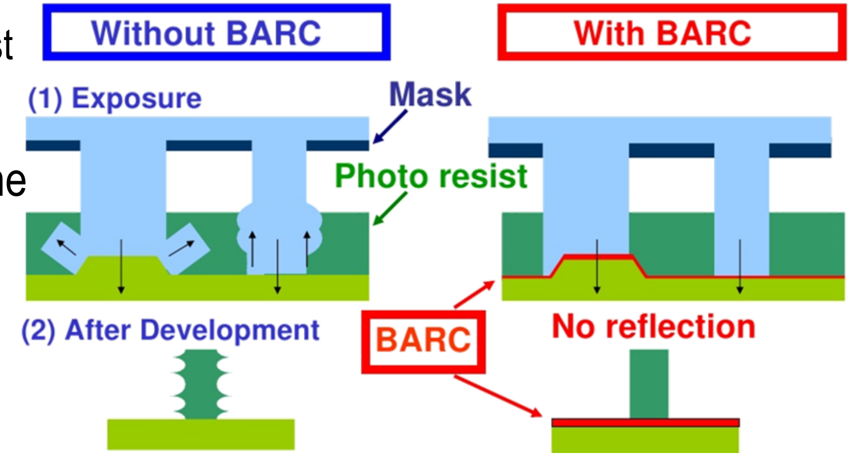


  - Resist stripping
    - Avoid too high hard-bake temperatures
    - For dry etching:
      - Avoid very long exposure to (very) energetic ions
      - Remember to do oxygen plasma etching after dry etching
  - Etch selectivity
    - For wet etching
      - HF might diffuse into resist
      - Wet solutions might decrease adhesion
      - Longer hard-bake

http://www.microchemicals.com/technical_information/TroubleShooter_EN.pdf

Main issues

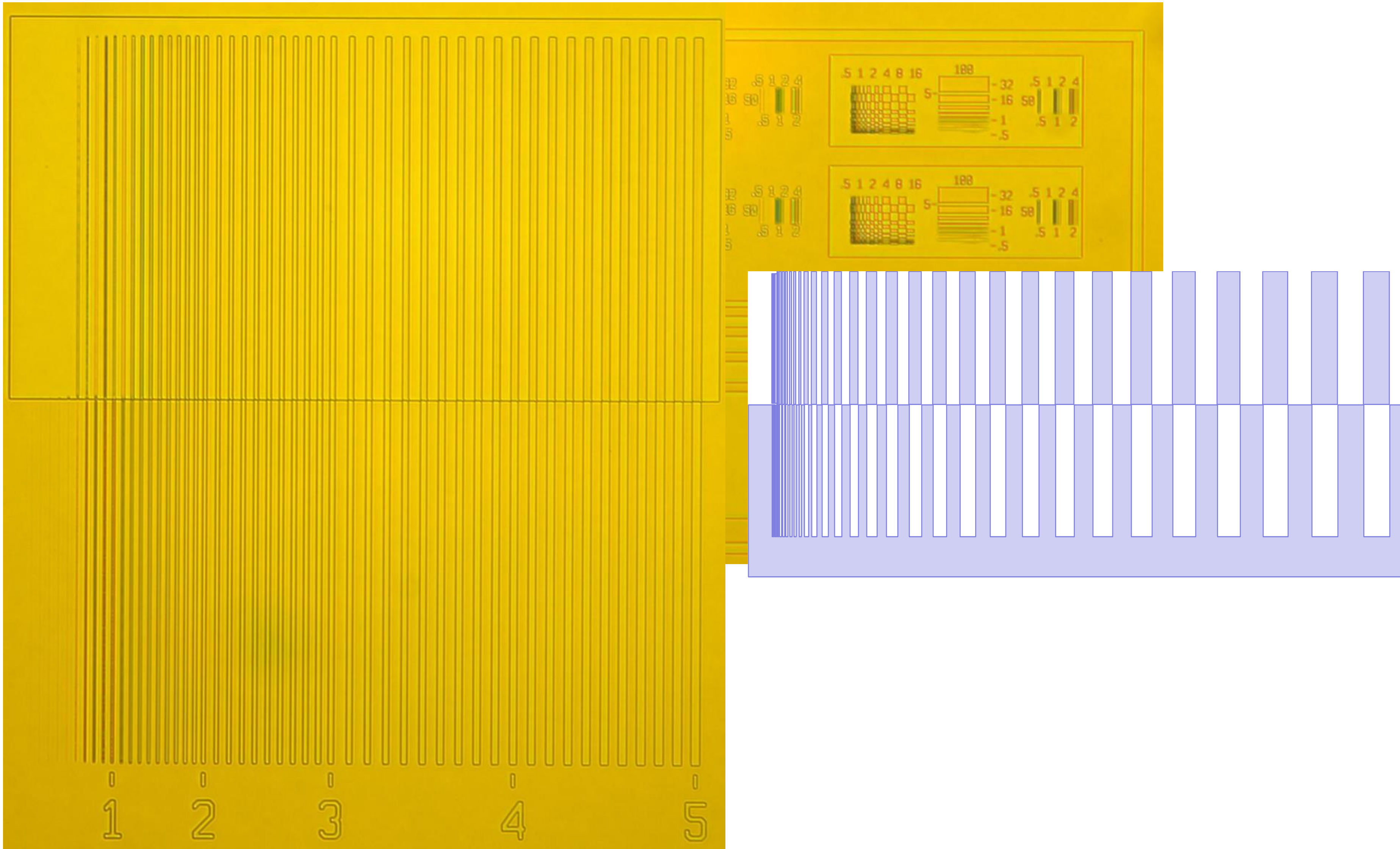
- Exposure
  - Reflectance of substrate
    - Pay special attention to
      - Transparent substrates → Create opaque backside
      - Metal substrates → Bottom Anti-Reflective resist
  - Wavelength of light
    - Always check when changing resist or machine
  - Hydration of resist
    - Some time between coating and exposure
    - Critical for thicker resist layers



  - Always perform exposure test
    - How to make sure that the dose is the right one?

http://www.microchemicals.com/technical_information/TroubleShooter_EN.pdf

Exposure test



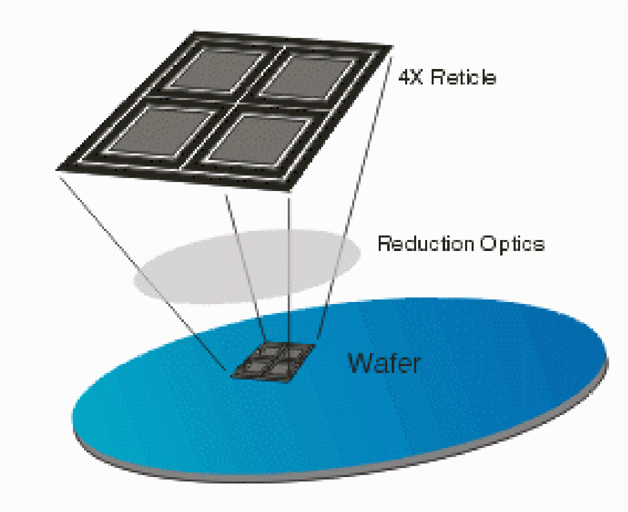
Main issues

- Development
  - Substrate damage
    - Typically developers are –OH based
      - Damaging of Al, Si, etc.
      - This is not very important if the material is going to be removed later
  - Overdevelopment
    - Developing more than once might cause a reduction of the resist dimensions
- Resolution limit (minimum dimensions)

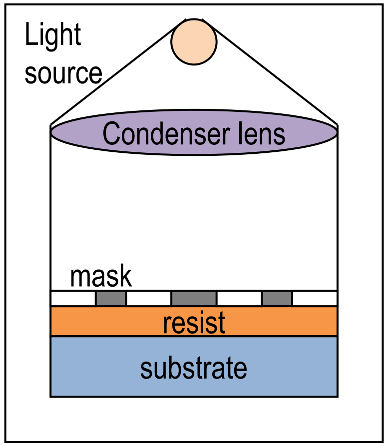
http://www.microchemicals.com/technical_information/TroubleShooter_EN.pdf

Illumination methods and resolution limits

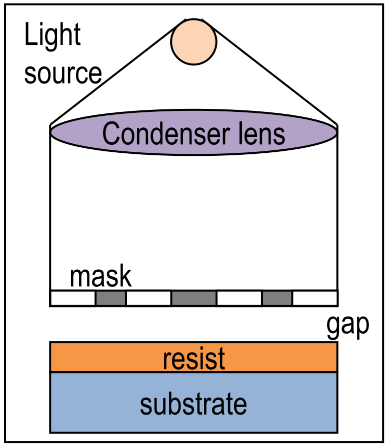
- 3 methods:
  - Contact
  - Proximity
  - Projection
- Key issue: minimum feature size (MFS)
  - Illumination method
  - Illumination wavelength
  - Materials of optical system
  - Resist used



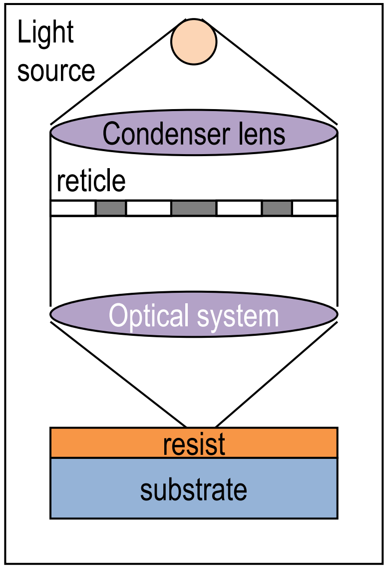
Contact



Proximity

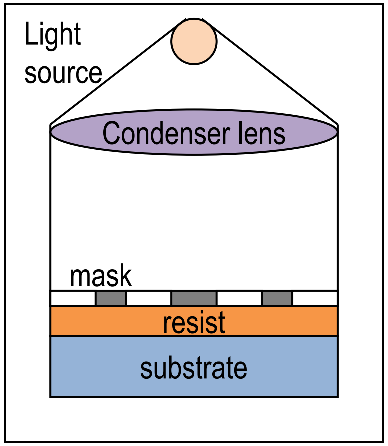


Projection



Illumination methods and resolution limits

Contact

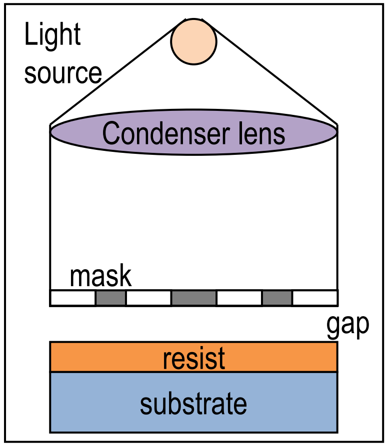


$$MFS = \sqrt{d \cdot \lambda}$$

$d = resist\ thickness$

$\lambda = wavelenght$

Proximity



$$MFS = \sqrt{(d + g) \cdot \lambda}$$

$d = resist\ thickness$

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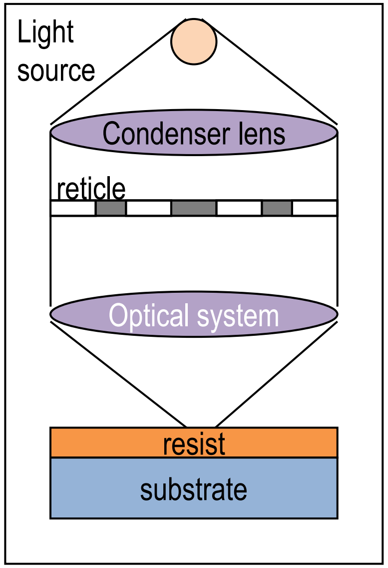
$g = gap$

Projection



$$MFS = k_1 \cdot \lambda / NA$$

$NA = Numerical\ Aperture$

$\lambda = wavelenght$

$k_1 = 0.5 - 0.9$

- Reduce MFS
  - … by reducing λ

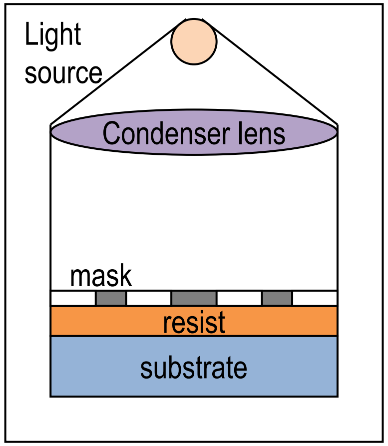
Exposure wavelength and light sources

Time

Wavelength [nm]	Source	Range
436	Hg arc lamp	G-line
405	Hg arc lamp	H-line
365	Hg arc lamp	I-line
248	Hg/Xe arc lamp, KrF excimer laser	Deep UV (DUV)
193	ArF excimer laser	DUV
157	F2 laser	Vacuum UV (VUV)
~ 10	Laser-produces plasma sources	Extreme UV (EUV)
~ 1	X-ray tube, syncrotonon	X-Ray

Illumination methods and resolution limits

Contact



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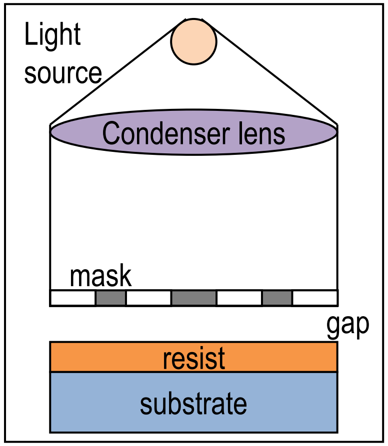

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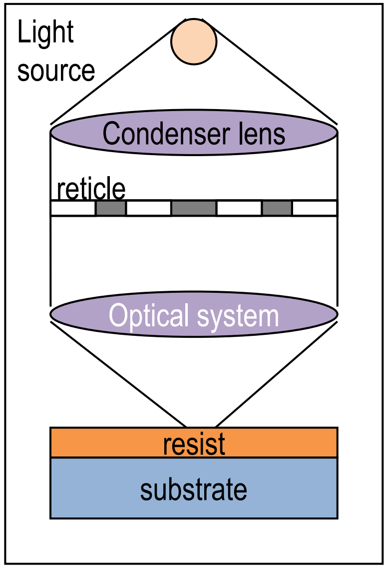

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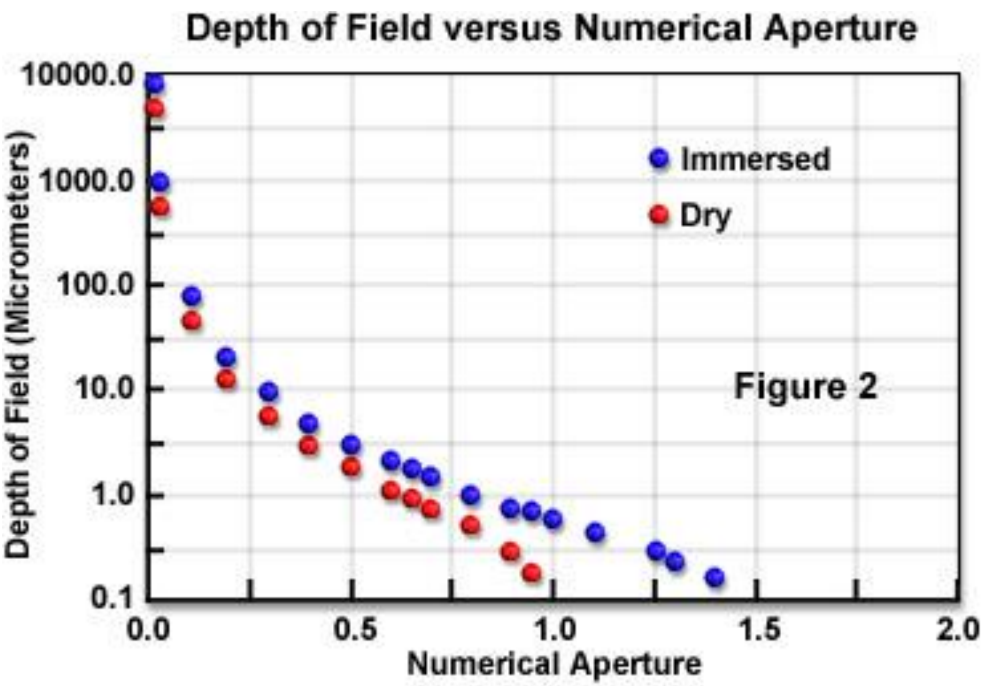
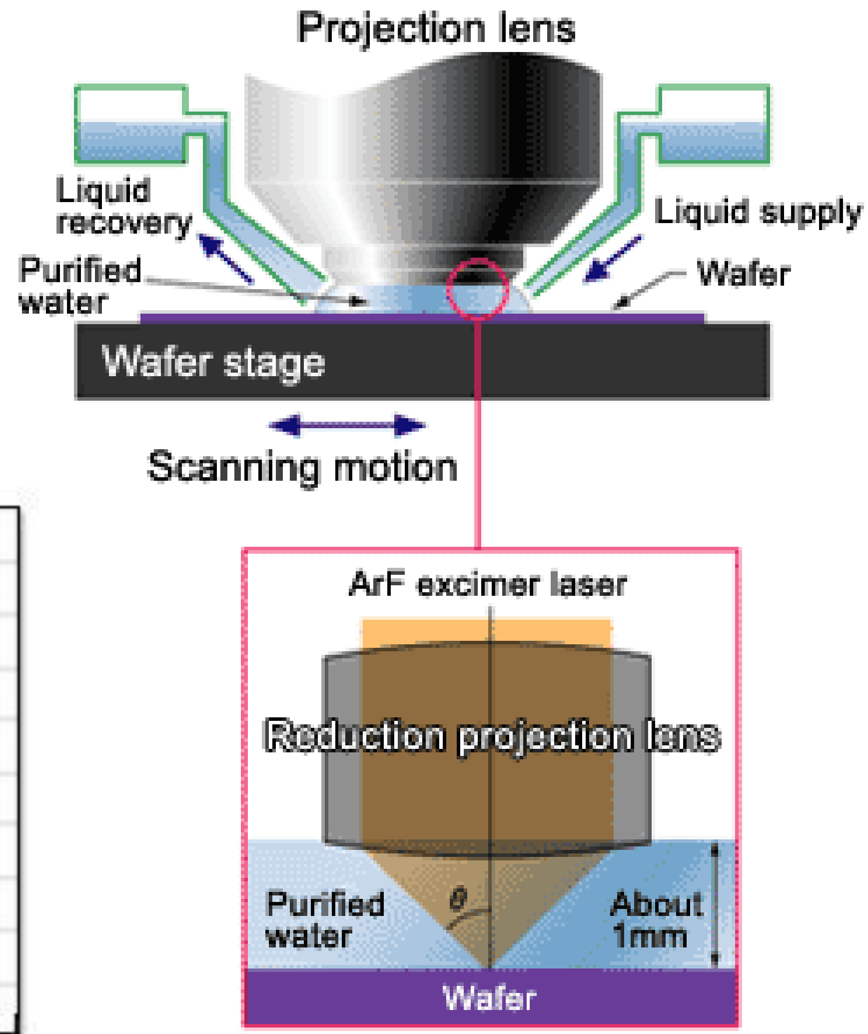
- Reduce MFS
  - … by reducing λ
  - … by increasing NA

Immersion lithography

- $NA = n \cdot {}^{D}/_{f}$
  - n is refractive index
  - D is lens diameter
  - f is focal length
- $n > 1$
  - $NA \nearrow, Depth\ of\ Field \nearrow$





Illumination methods and resolution limits

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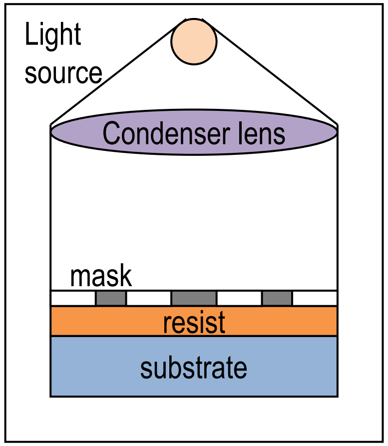

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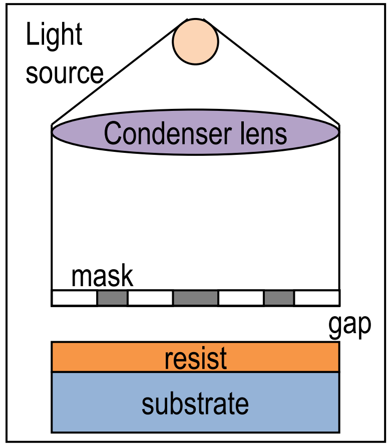

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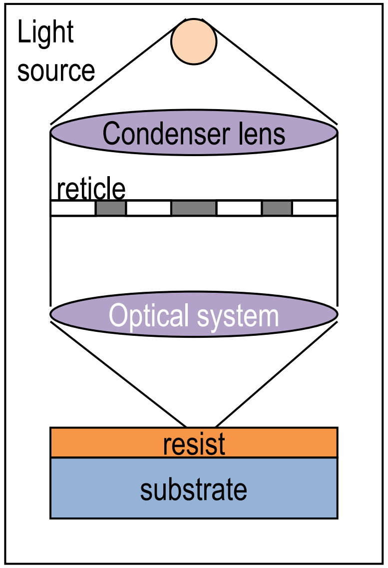

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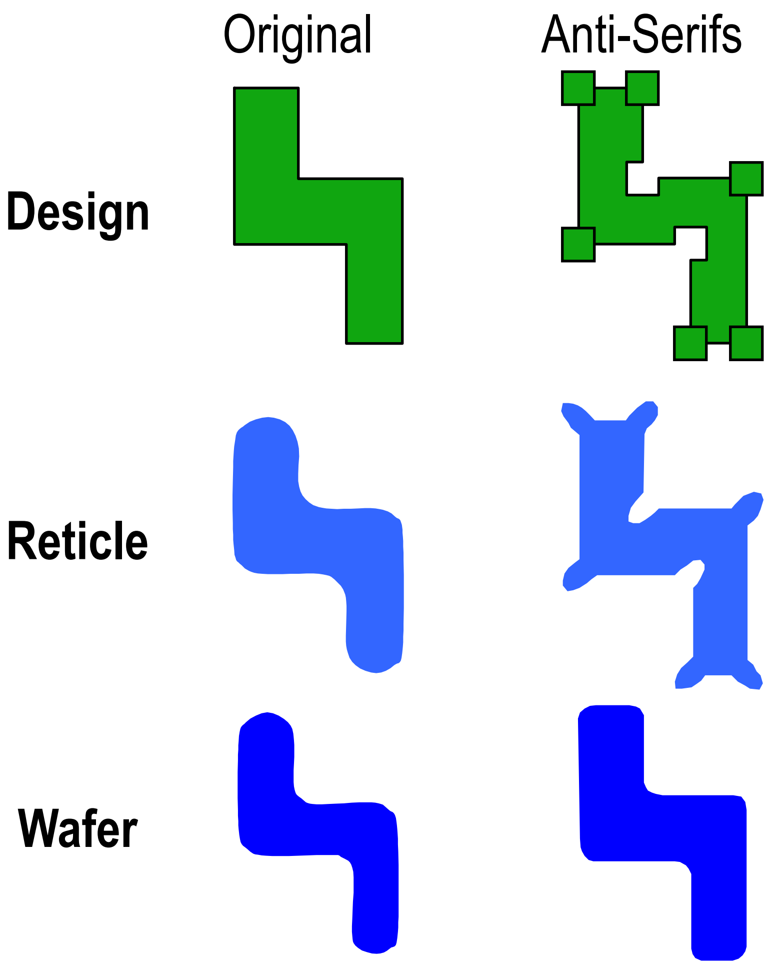
- Reduce MFS
  - … by reducing λ
  - … by increasing NA
  - … by reducing k_1

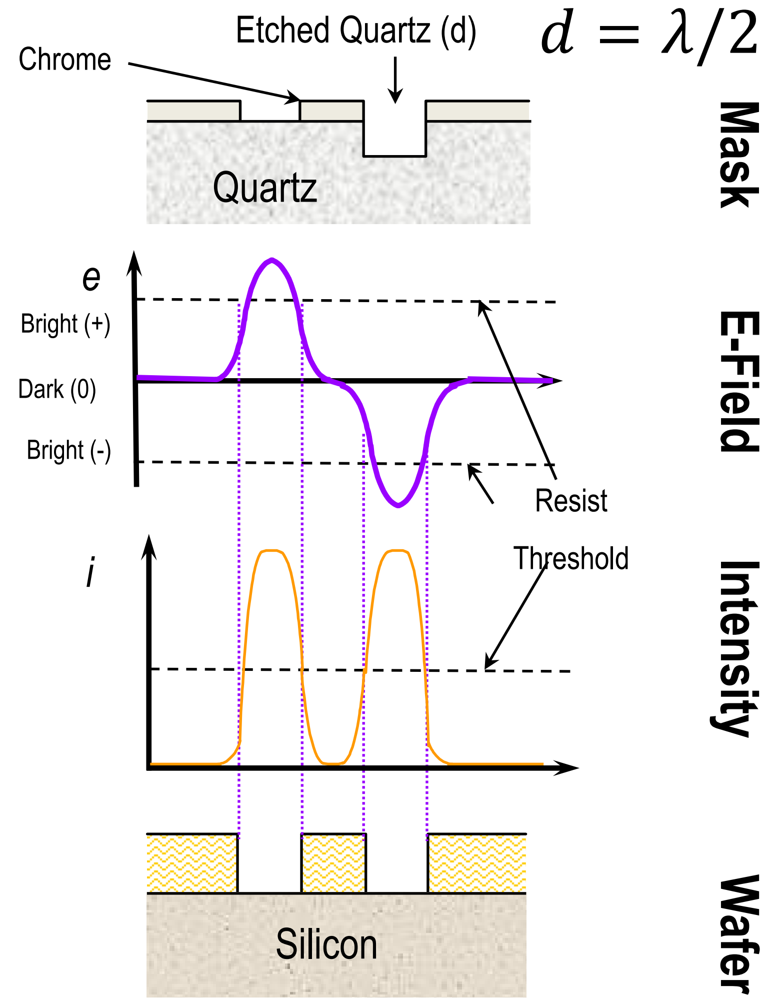
Improving k_1

OPC - Optical Proximity Correction



PSM – Phase Shift Mask

$$d = \lambda/2$$



Using I-line Hg Lamp, 1 µm thick resist: What is the MFS when using a mask in contact?

A. 604 nm
B. 253 nm
C. 877 nm
D. 1021 nm
E. 545 nm

$$MFS = \sqrt{d \cdot \lambda}$$
$$d = resist\ thickness$$
$$\lambda = wavelenght$$

$$MFS = \sqrt{(d + g) \cdot \lambda}$$
$$d = resist\ thickness$$
$$\lambda = wavelenght$$
$$g = gap$$

$$MFS = k_1 \cdot \lambda / NA$$
$$NA = Numerical\ Aperture$$
$$\lambda = wavelenght$$
$$k_1 = 0.5 - 0.9$$

With an optimized optical system, NA=1.5, λ for 100 nm MFS?

A. 100 nm
B. 200 nm
C. 300 nm
D. 400 nm
E. 600 nm

$$MFS = \sqrt{d \cdot \lambda}$$
$$d = resist\ thickness$$
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$$MFS = \sqrt{(d + g) \cdot \lambda}$$
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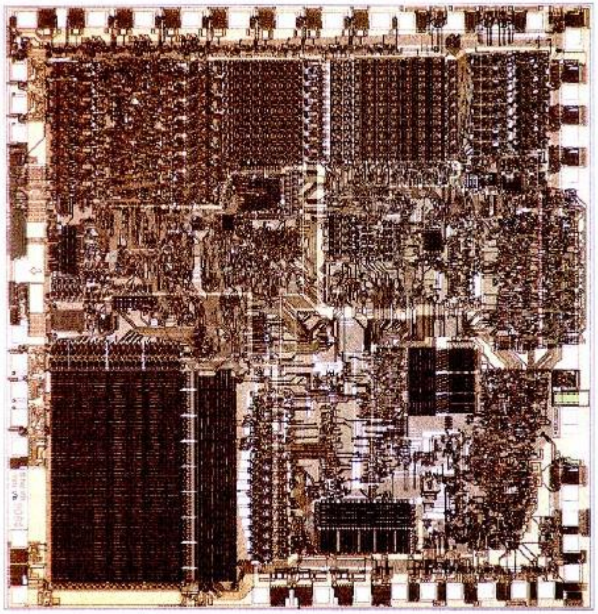
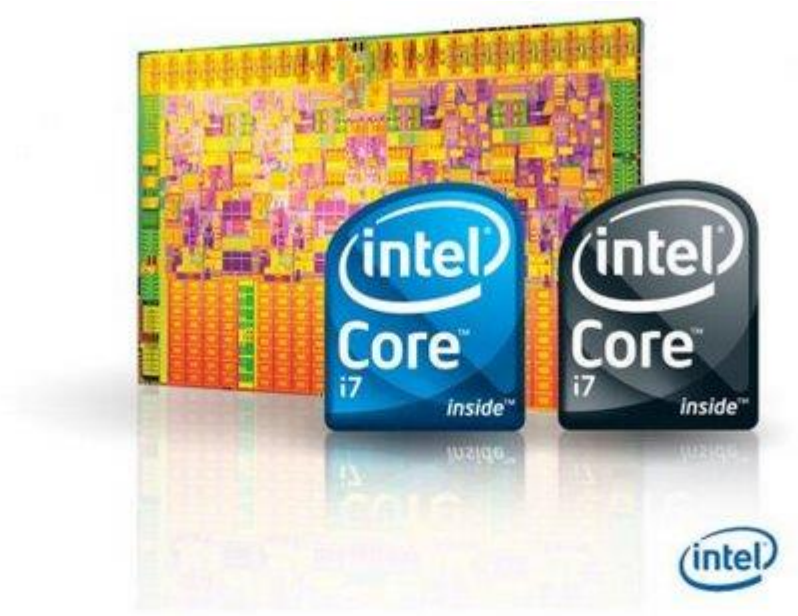
Lithography (III)

CMOS evolution

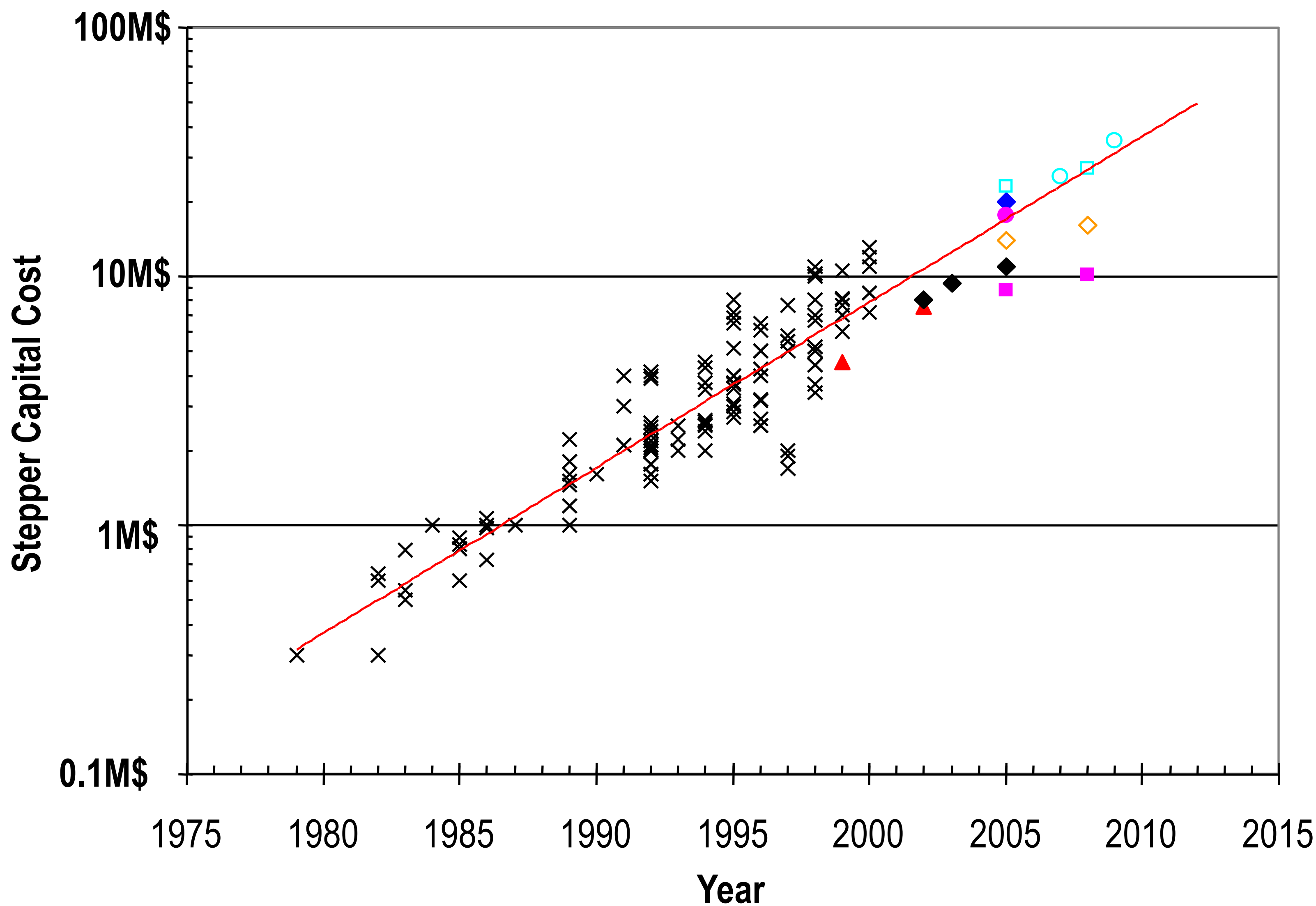


Intel 8088
3 μm node
29000 Transistors



Core i9 – 9th gen
14 nm node
7 Billion Transistors

Evolution of cost



Another way to reduce λ

- Use of electrons instead of photons to irradiate the resist
- Energy of accelerated electrons is

$$E = eV = \frac{1}{2}mv^2 = \frac{p^2}{2m}$$

- De Broglie wavelength is (V in kV)

$$\lambda = \frac{h}{p} = \frac{h}{mv} = \frac{h}{\sqrt{2mE}} \approx \frac{0.38\text{Å}}{\sqrt{V}}$$

- No limitted by diffraction – Game changing!

Types of lithography

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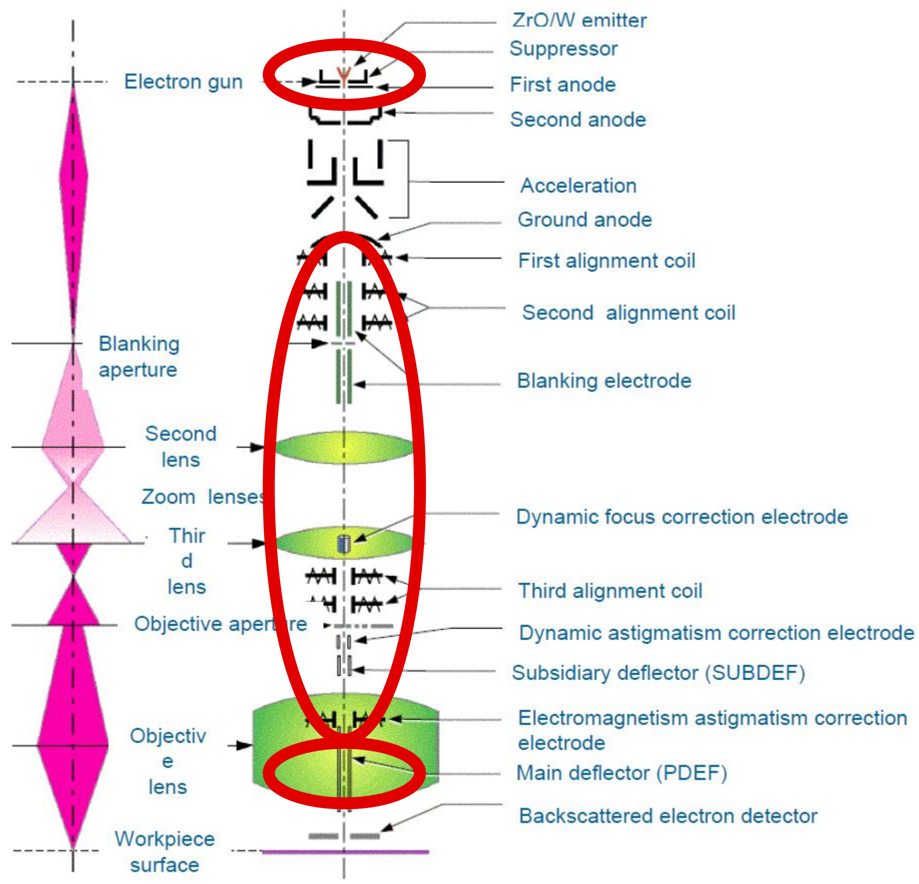
- Scanning Probe Lithography (SPL)
- Nano Stencil Lithography (nSL)
- Directed Self Assembly Lithography (DSAL)
- …

EBL – Steps

- Preparation of design and conversion
- Coating
- Exposure
- Development

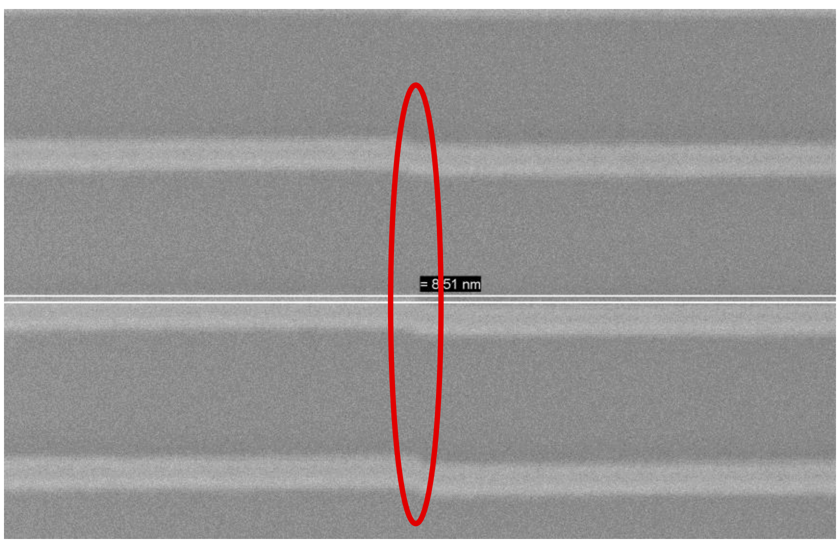
EBL System #1 - Column

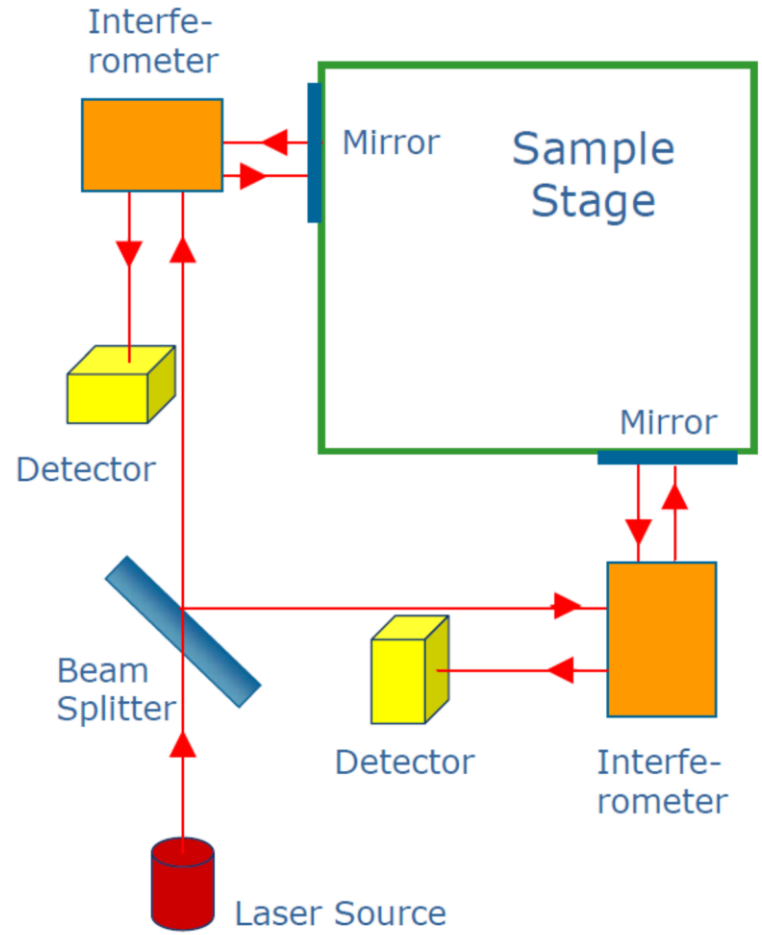
- The *column* is the most important component of an EBL system
- Composed by:
  - Electron emitter
  - Lenses
  - Deflector
- MFS determined by
  - Aberrations in electron optics
  - Electron-Solid interactions (scattering)



EBL System #2 - Stage

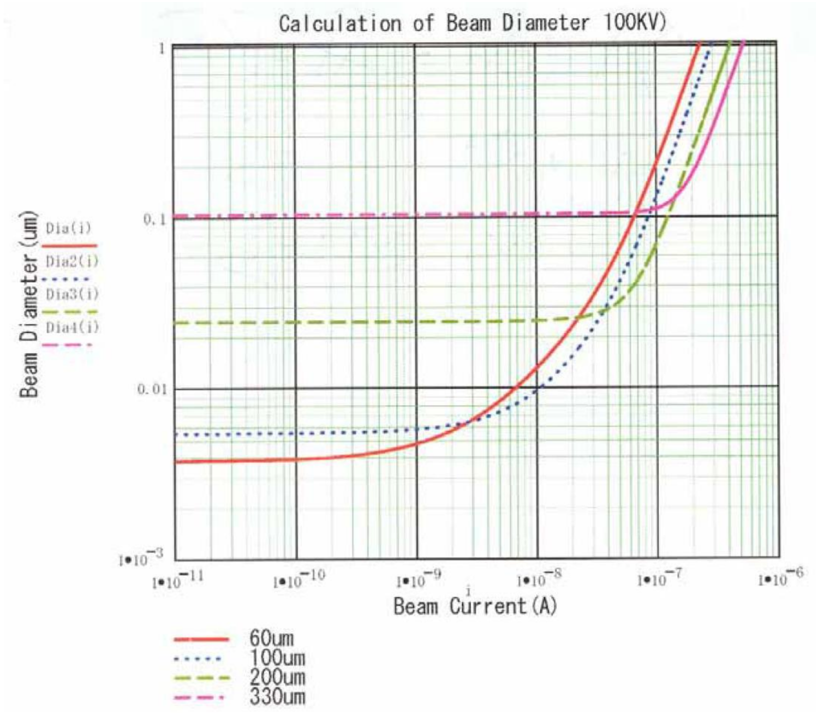
- Deflector can only reach an area of $\sim 200x200\mu m^2$
- Beyond that, the *stage* needs to be moved
  - Very accurate position control is needed
- Using two Michelson interferometers:
  - Minimum resolution <1 nm
  - Repeatability <<50 nm
  - Stitching <20 nm





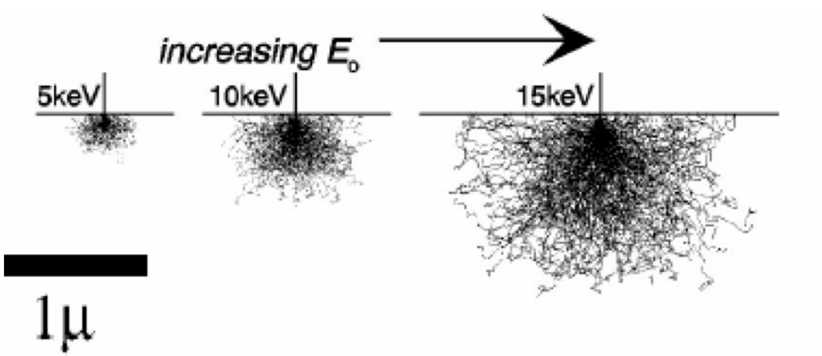
Resolution limits – Aberrations

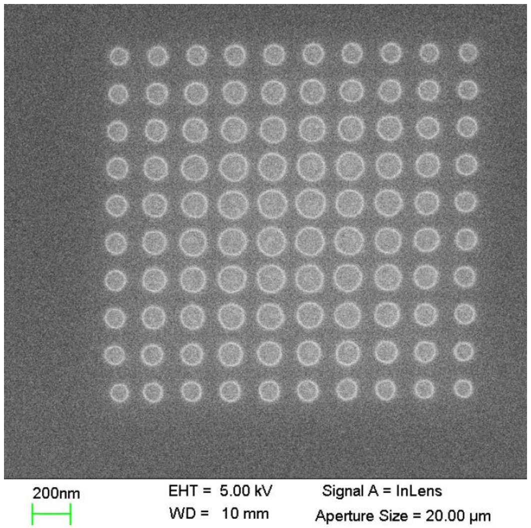
- Electron lenses are not as good as optical ones
- Beam diameter on the wafer increases with increasing current
  - 1-5 nm minimum beam diameter
- Larger current implies less writing time (two reasons)



Resolution limits – Electron-Solid interaction

- As electrons enter the solid, they start scattering – pattern broadens
- Forward scattering
  - Beam broadens when it enters the resist
  - Minimizes for high energy and thin resist
- Back scattering
  - In the substrate, beam broadens much more, some electrons return into the resist
  - These electrons cause additional exposure → **Proximity effect**
  - Increases for high energy of the beam





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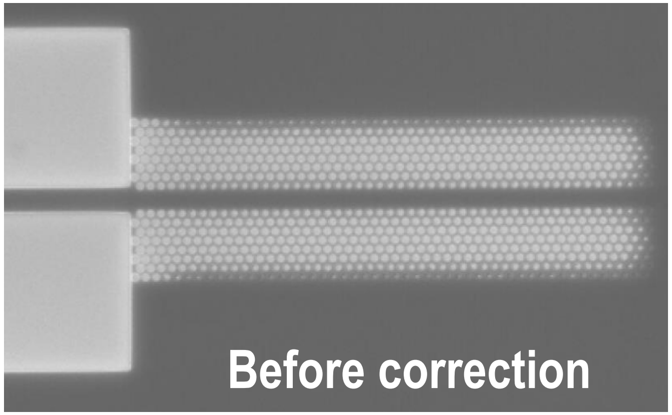
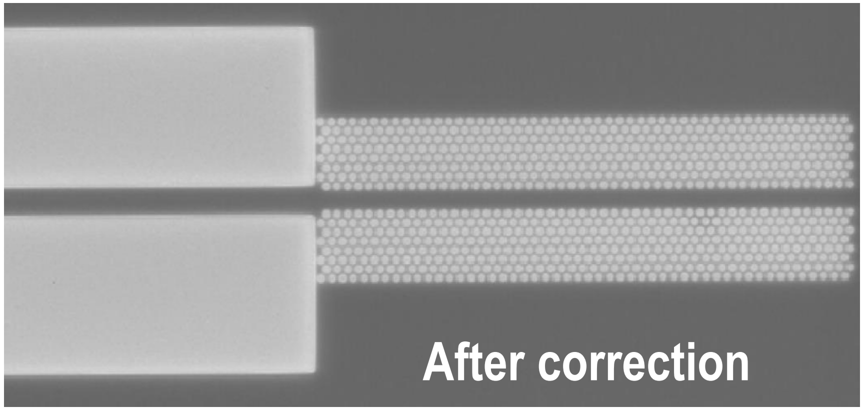


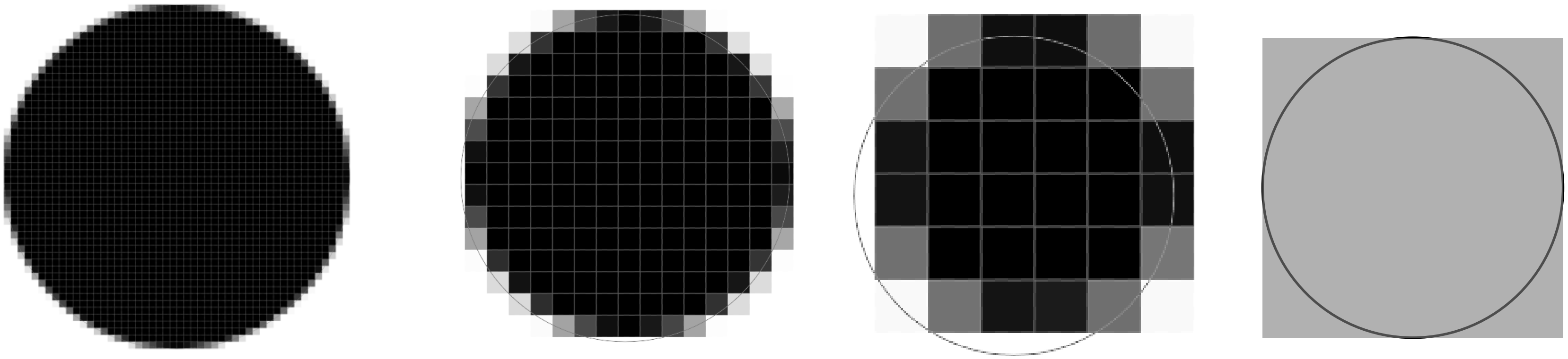


EBL Resists

- Positive
  - PMMA
    - Very well known
    - Good for lift-off (different MWs available)
    - Bad as an etch-mask
    - $\sim 100\ \mu C/cm^2$
  - ZEP
    - Very good as an etch-mask
    - $\sim 10\ \mu C/cm^2$
- Negative
  - HSQ
    - Good as an etch-mask
    - Very high resolution
    - $\sim 500\ \mu C/cm^2$

Pattern generator

- A software is required to convert a CAD file into an EBL pattern
  - Based on MFS we decide the electron beam diameter
  - This helps us determine the “pixel” size used to “pixelize” our CAD design



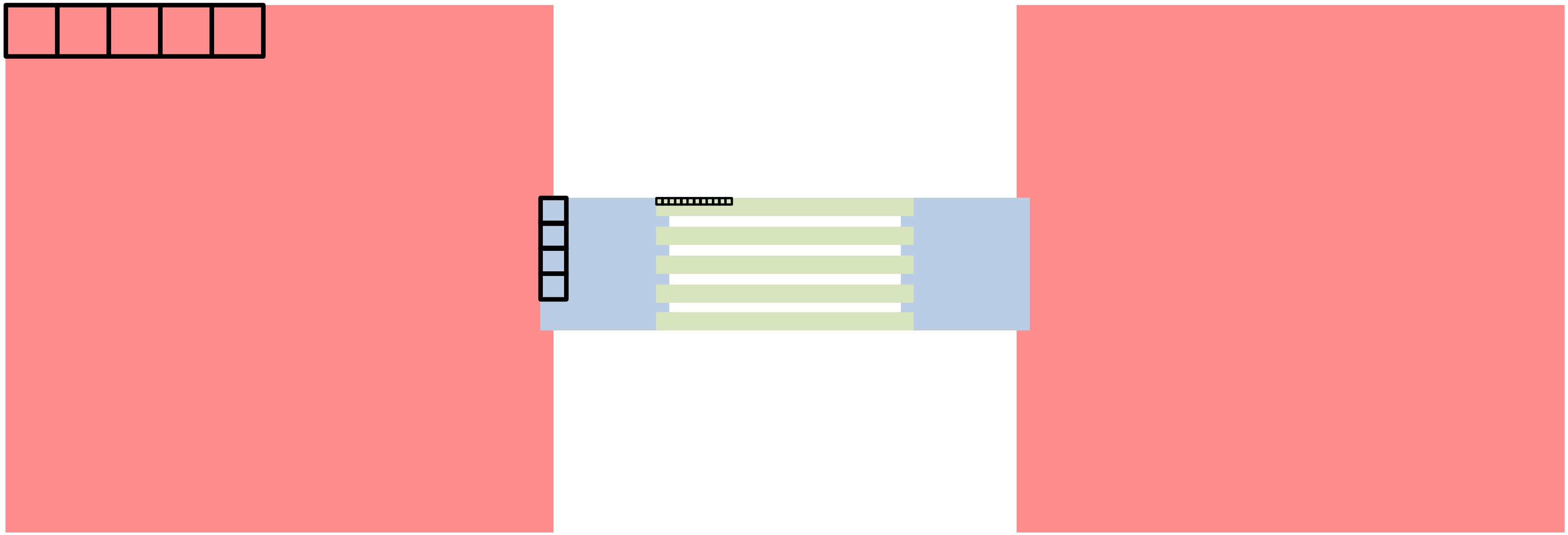
  - If pixel<beam – Overlapping
  - Then we decide the beam current, aperture diameter and dose
- Dose depends on resist, substrate, pattern, pixel size, overlapping, etc.
- Exposure time: $Time = \frac{Dose \cdot Area}{Current}$
- Actual writing time is usually dominated by stage speed
  - Beam deflection $\sim$ 50MHz, Stage movement $\sim$ 1Hz

Pattern generator – Case Study

- How to write something like this using EBL?

Pattern generator – Case Study

- How to write something like this using EBL?
  - Split of the design in 3 layers
  - It is important to leave some overlap to correct for possible misalignments
  - Each layer can have a different pixel size
  - Like this we optimize (1) writing time and (2) resolution



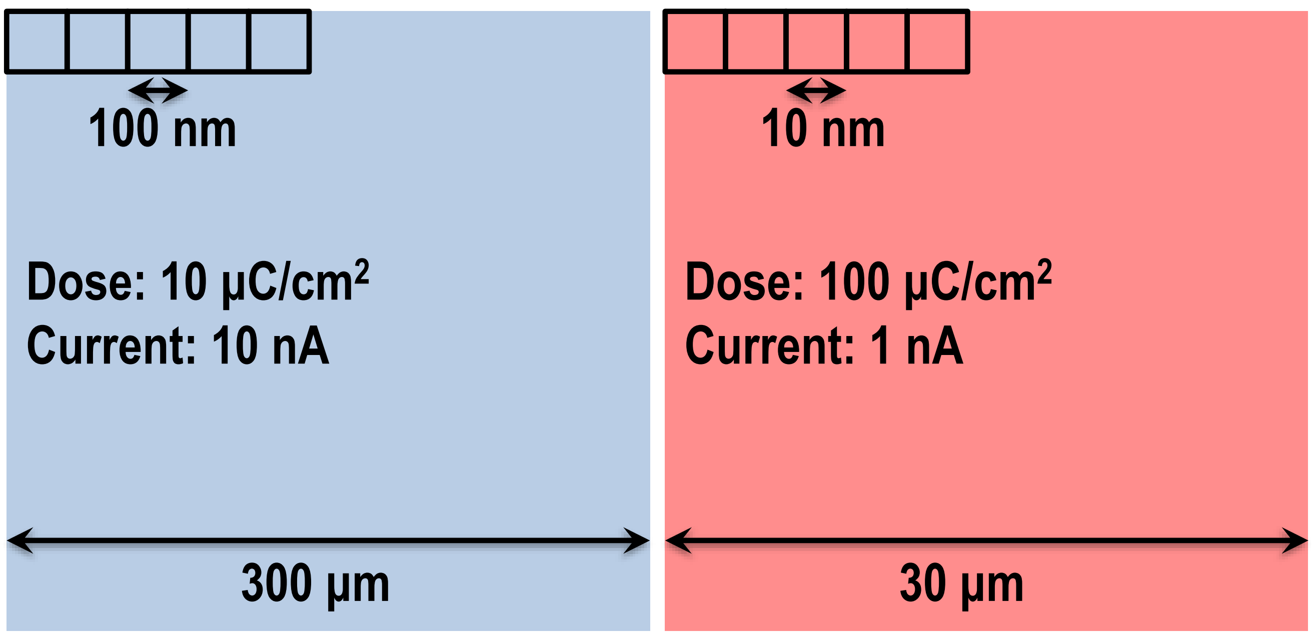
How do we get better resolution?

A. Using a **high** energy beam
B. Using a **low** energy beam

Which pattern takes longer to write?

A. Case Blue

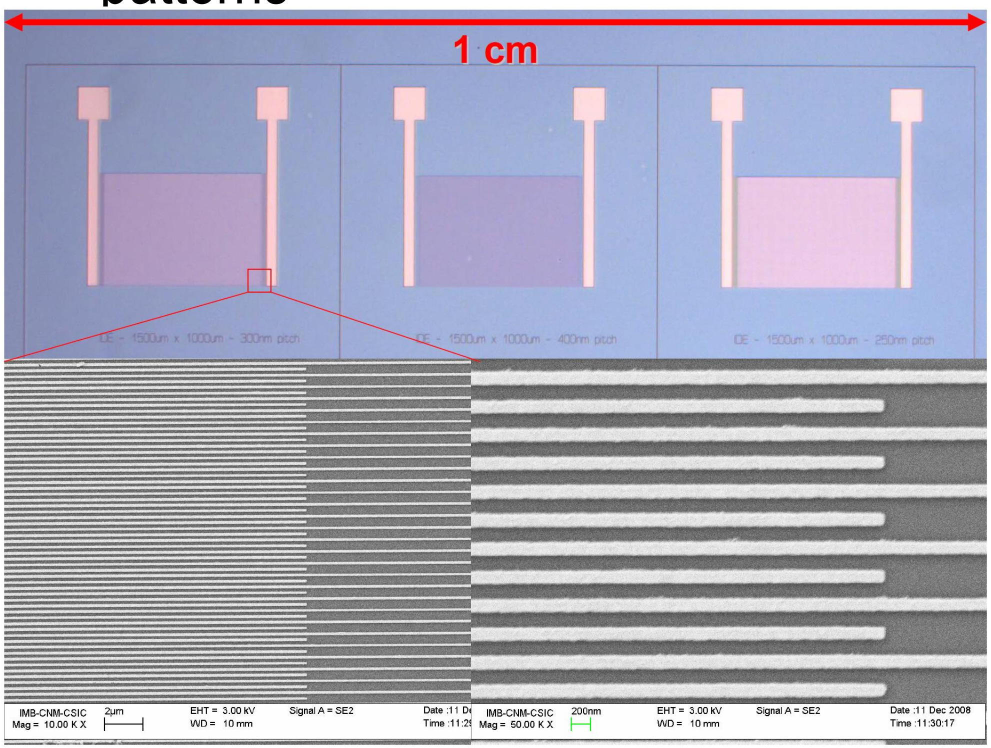
B. Case Red

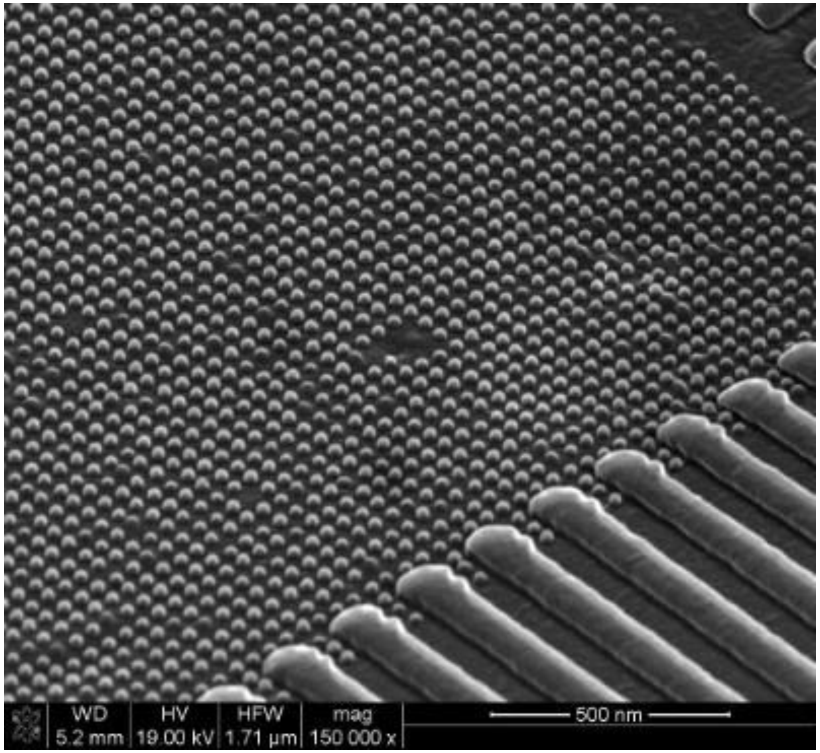


Case Blue **Case Red**

Main limitation of EBL

- EBL is a serial process
- High resolution and accuracy, but takes a long time to write dense patterns





OK!

Too much time!

Types of lithography

- Optical lithography
- Electron Beam Lithography (EBL)
- **Nano Imprint Lithography (NIL)**
- Scanning Probe Lithography (SPL)
- Nano Stencil Lithography (nSL)
- Directed Self Assembly Lithography (DSAL)
- …

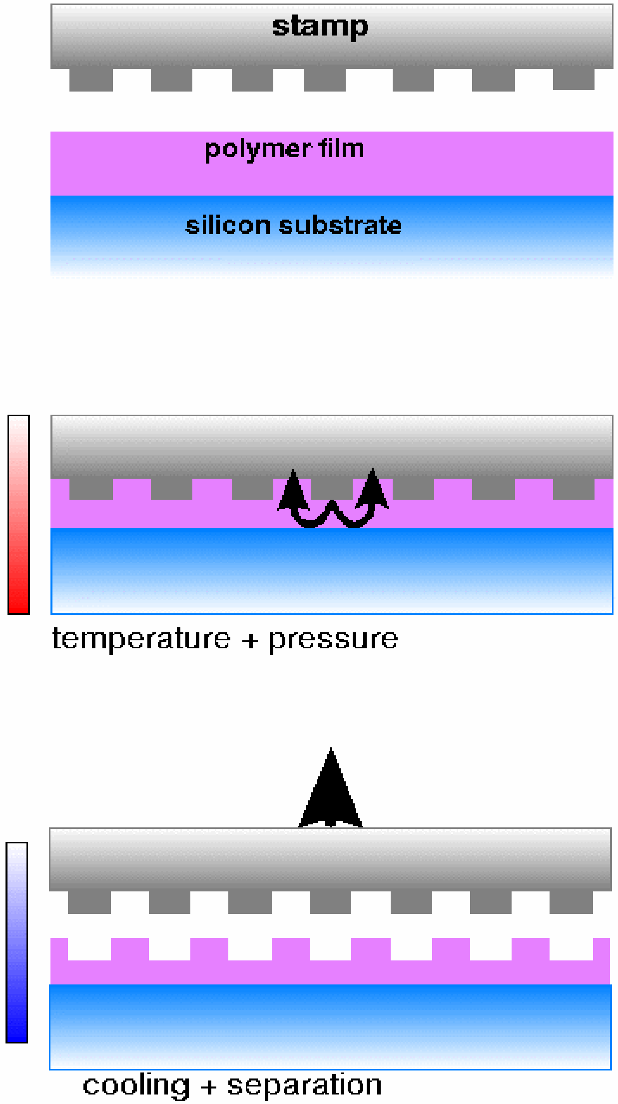
NIL - Steps

- Stamp fabrication
- Coating
- Imprint Process
- De-scum

Imprint process

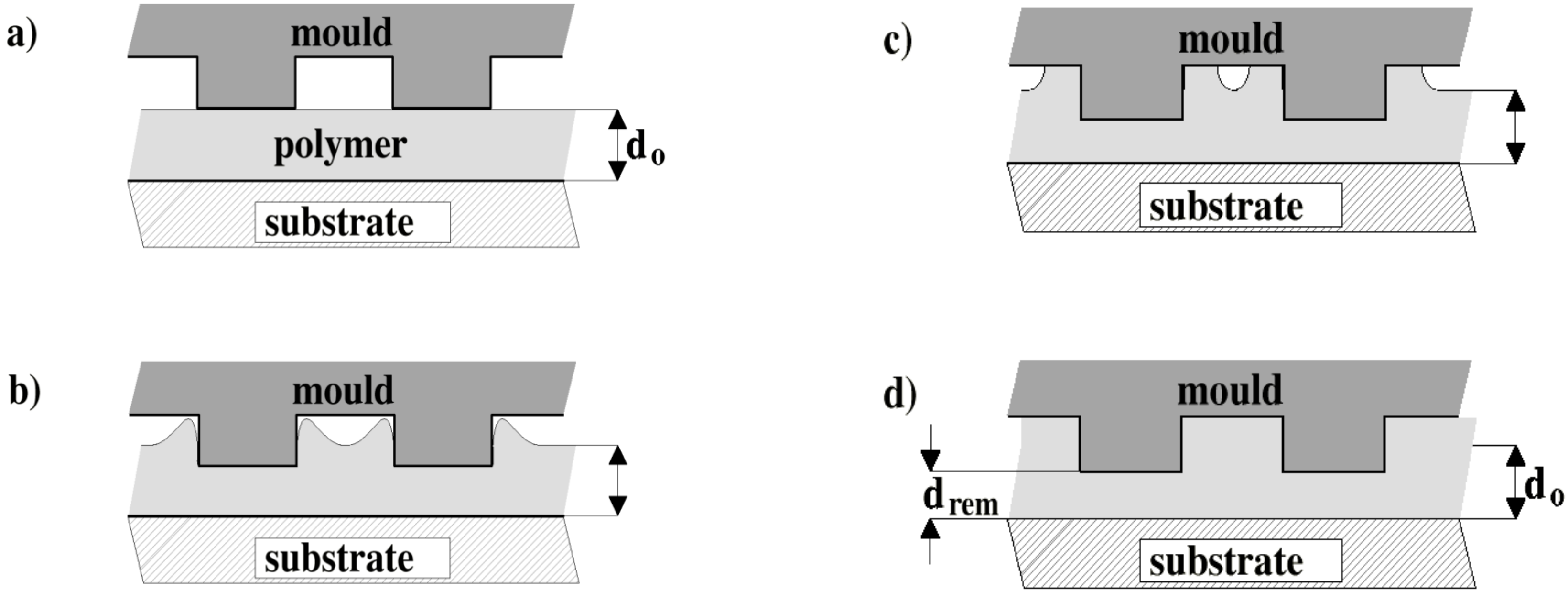
- 1. Heat to $T>T_g$
  2. Bring stamp & sample into contact
  3. Apply pressure
  4. Cool down
  5. Separation at $T<T_g$

- Relatively simple process
- MFS ~10 nm
- Low cost
- Scalable to wafer size

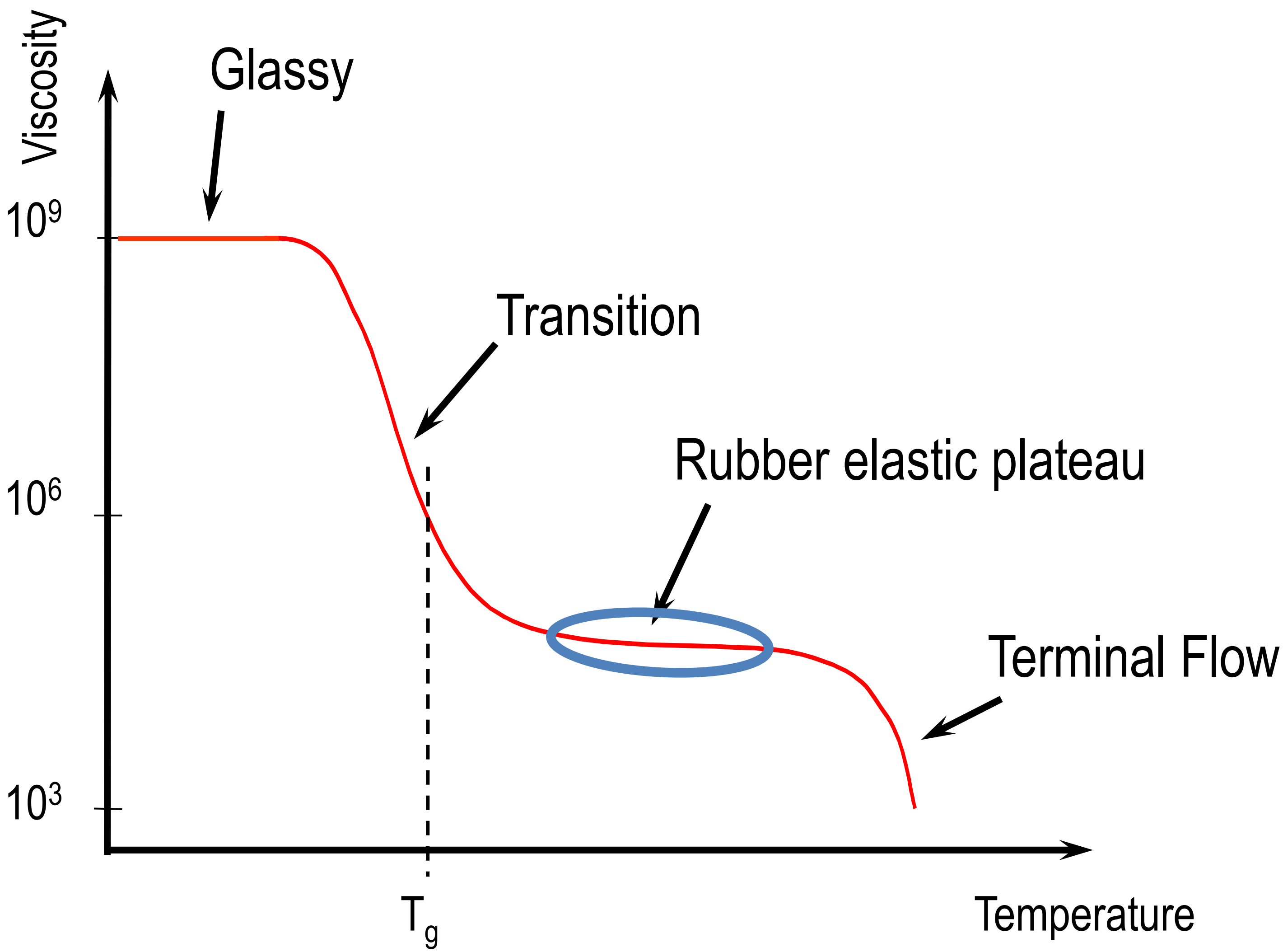


Imprint process

- Originally contact area is only @ elevated structures
- Polymer is displaced
- In the end, contact area is much larger
  - Very large force is required to cause vertical displacements
  - There is always a thin resist layer remaining (residual layer)

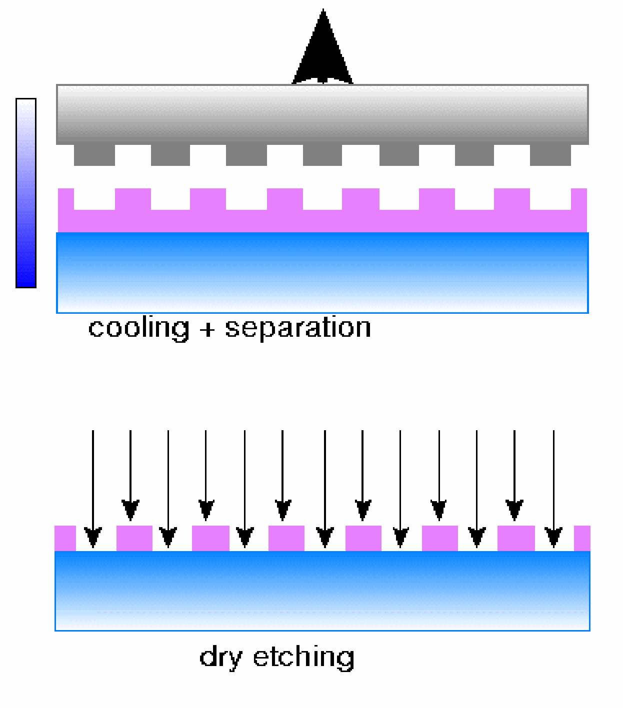


Imprint Process & Resist properties



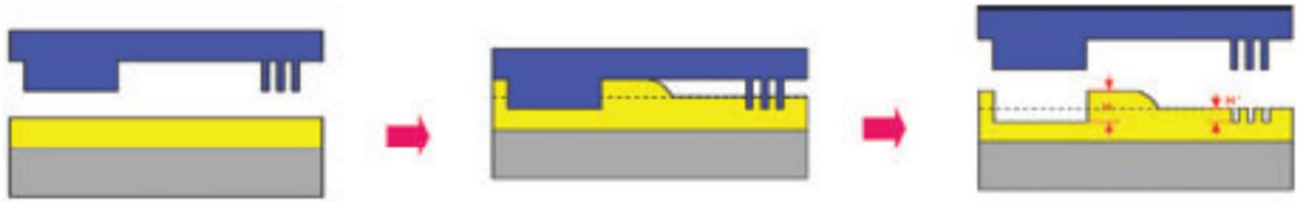
Residual layer removal

- After releasing the stamp
  - There is always a thin layer of polymer remaining everywhere
- Before continuing with any process, this needs to be removed
  - By a soft *dry etching*

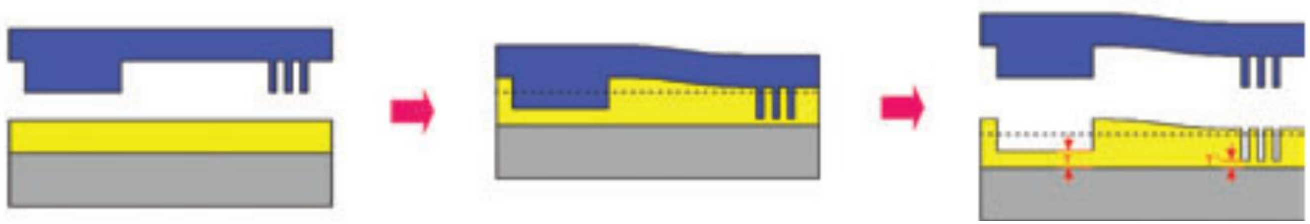


Challenges in NIL

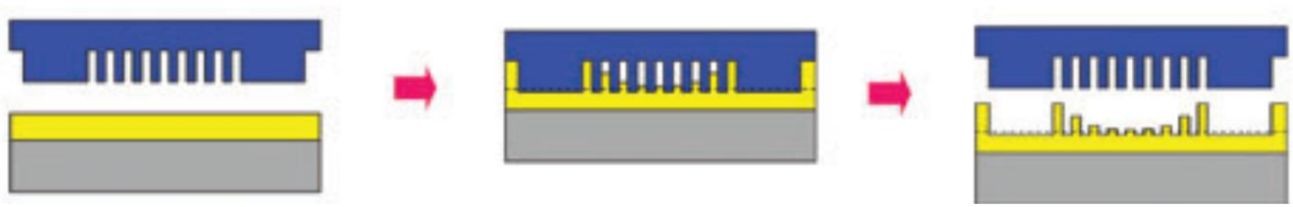
- Important issues come up when patterning structures of very different dimensions:
  - Isolated structures: Insufficient flow



  - Inhomogeneous pressure distribution

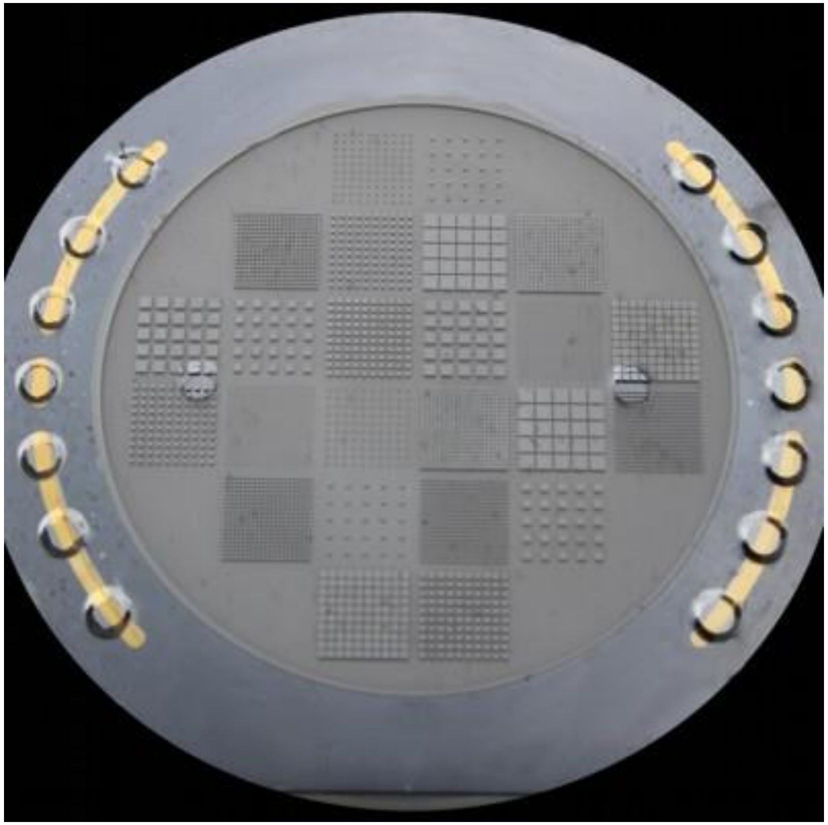


  - Insufficient displacement of the polymer



Stamp fabrication

- As for Optical Lithography, an EBL is needed to create the first master
  - Which you can later replicate by
    - NIL
    - Electroplating
    - Polymer casting
    - etc.

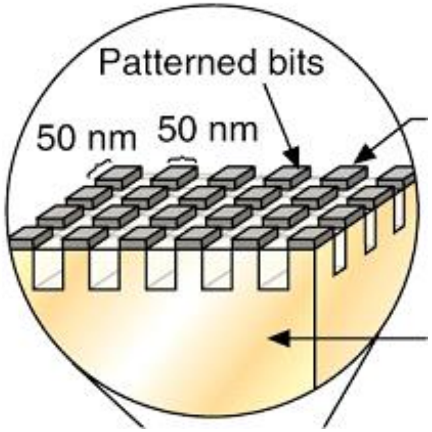


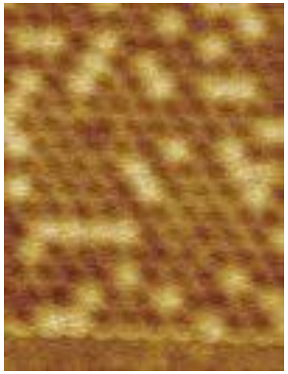
- Materials:
  - Silicon
  - Metal
  - Polymer

Main Areas of Impact

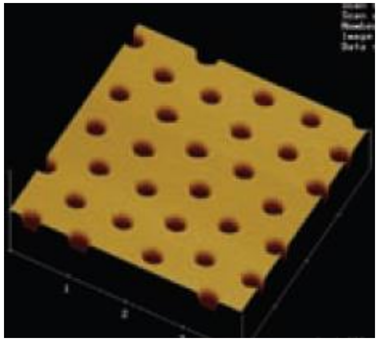
- Applications requiring pattern transfer over large areas with high throughput
- Cost-efficient applications
- Layers not requiring alignment
- Laboratory-scale exploratory work on nanotechnology
- Patterning of functional materials

Patterned Magnetic Media

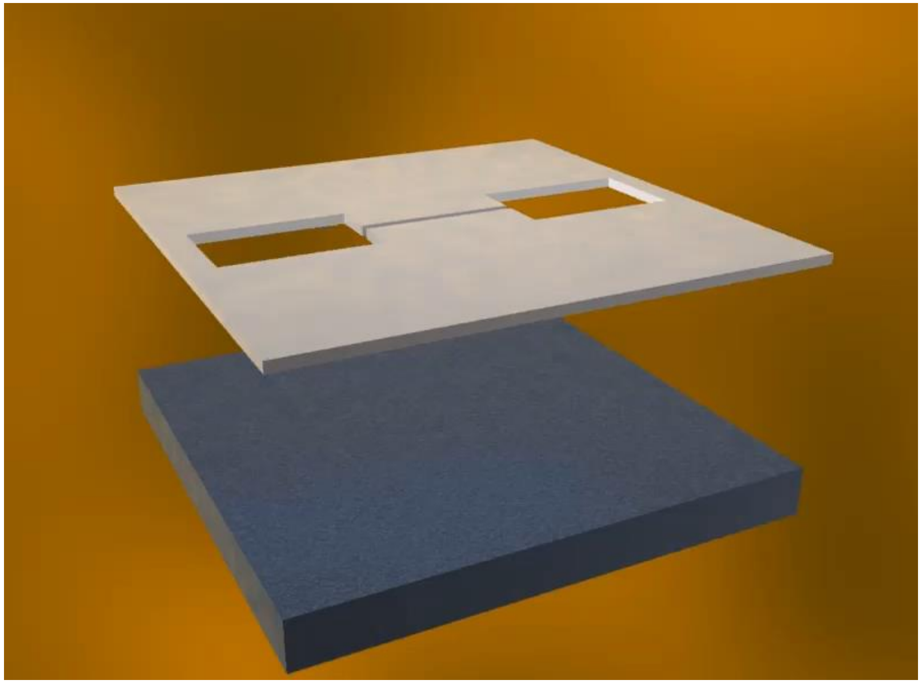




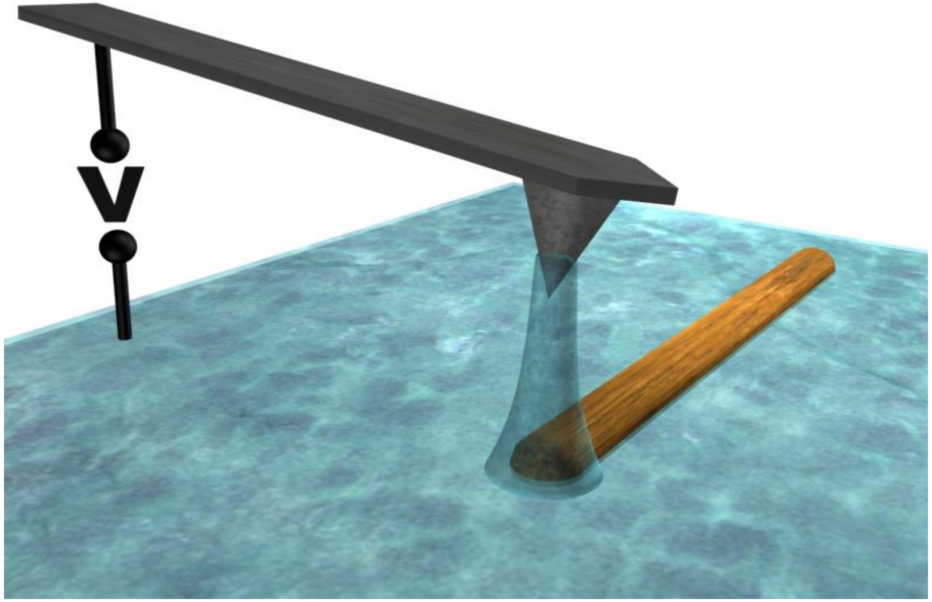
High Brightness LEDs



Many more methods up-and-coming...



Stencil Lithography



Scanning Probe Lithography

Summary table

Deposition

Implantation

TOP-DOWN

Etching

- Method to “draw” on the wafer
- Optical, EBL, NIL, …
- Best option depends on design, requirements and $$$

Lithography

Implantation

What and why?

- Ion implantation is the process which turns pure silicon into
  - P-type – Doping with ions from group III, e.g. Boron
  - N-type – Doping with ions from group V, e.g. Phosphorous, Arsenic

- This is necessary for the fabrication of transistors and diodes, and to control conductivity of Si

https://www.youtube.com/watch?v=V-U3v9QBPO4

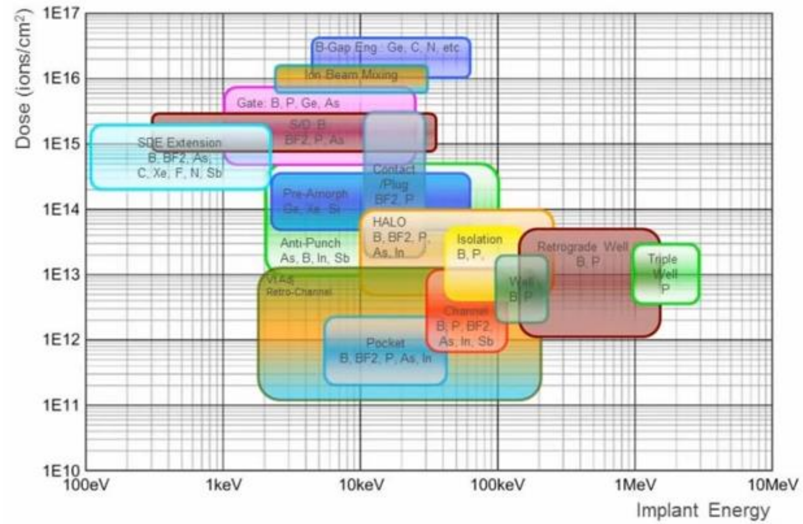
Steps

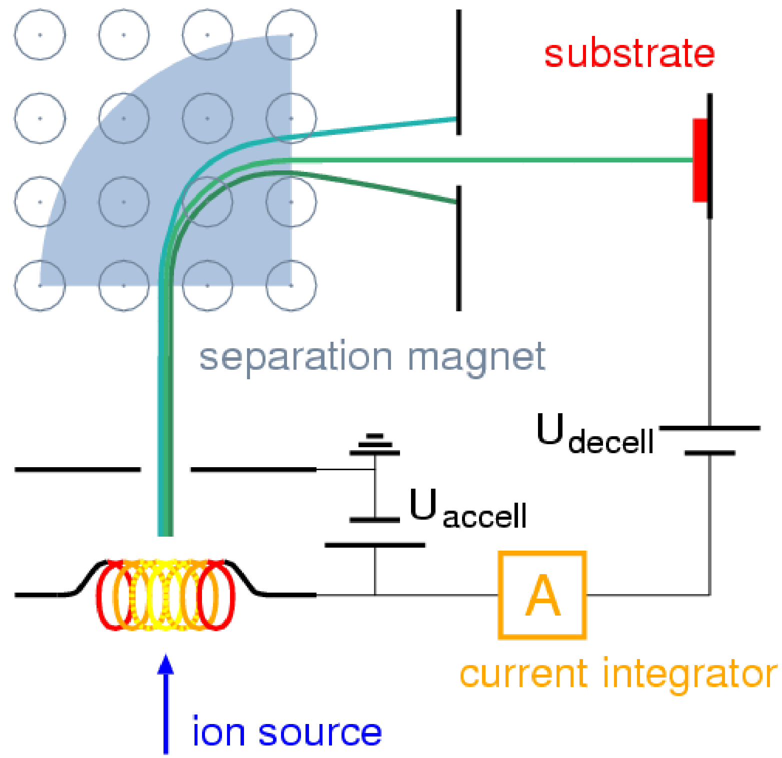
- Pattern is generated on the substrate via lithography
  - Mask can be resist, silicon dioxide, silicon nitride, etc.
- Ions are implanted in the wafer using a given energy & dose
- Annealing at high T is required to
  - “incorporate” the impurities into the lattice
  - correct defects that have been caused by the ion bombardment

Implanter

- Ions are generated and accelerated
  - Acceleration voltage sets up the energy of the implantation
- Magnetic lenses are used to filter out the unwanted ions
- The collimated ion beam reaches the wafer

- Two main parameters
  - Energy – determines the penetration depth
  - Dose – determines the concentration of ions





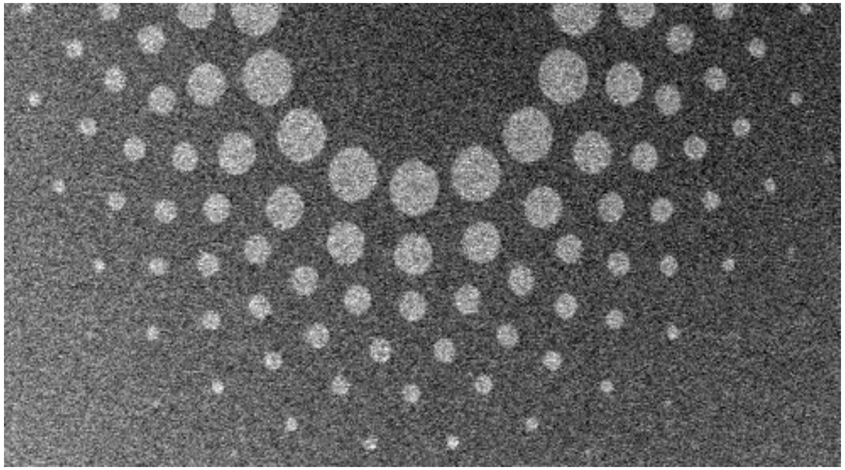
Annealing

- Two main parameters
  - Temperature
  - Time

- Challenge:
  - Loss of resolution due to diffusion of impurities
- Solution: Rapid Thermal Annealing
  - Enormous T ramps to get to >1000ºC in less than a second
  - Diffusion is then limited and nm dimensions can be kept

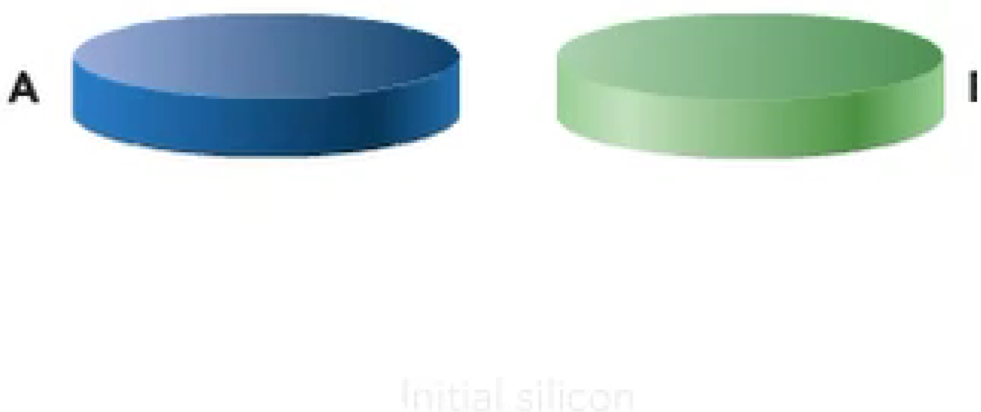
Keep in mind

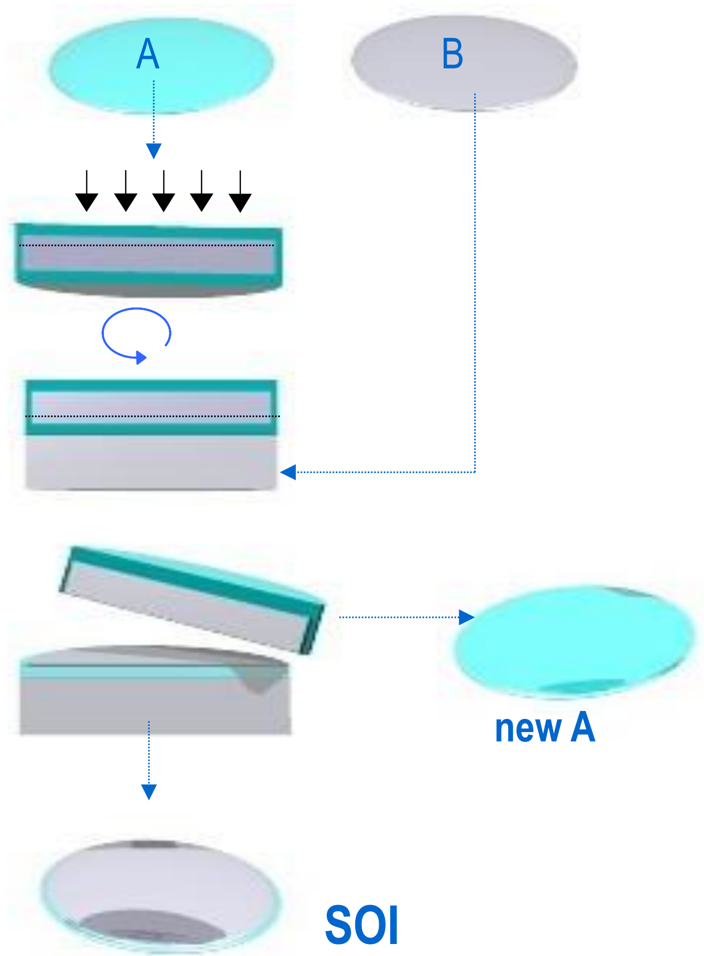
- After implantation and annealing
  - Once the mask is removed the material will look the same everywhere
  - It might be very challenging to locate your patterns on the substrate
- Tricks:
  - Pre-pattern substrate
  - "Develop" implanted regions – using etch rate dependence on doping level



Not only P/N doping

- Typical doping level in source/drain
  - $5 \cdot 10^{20} \mathrm{cm}^{-3}$, approx. 1:100 compared to Si atoms
- SOI Wafers – SmartCut® process
  - Oxidized wafer (A) & Initial silicon wafer (B)
  - Ion implantation – Hydrogen
  - Wafer Bonding
  - Splitting
  - Annealing and CMP touch polishing





Summary table

Deposition

Implantation

- Dope Si – transistors, etc.
- Generate new substrates – SOI
- Ion energy and dose
- Annealing is critical for “nano”

TOP-DOWN

Etching

Lithography

- Method to “draw” on the wafer
- Optical, EBL, NIL, …
- Best option depends on design, requirements and $$$

Deposition

Deposition

- Process to deposit/grow a thin film of material onto the substrate
  - As different types of materials are required, different techniques are used

- Spin coating
- Electrodeposition
- Thermal oxidation
- Chemical Vapor Deposition
  - LPCVD, PECVD, MOCVD, ALD…
- Physical Vapor Deposition
  - Sputtering, evaporation, MBE, PLD…

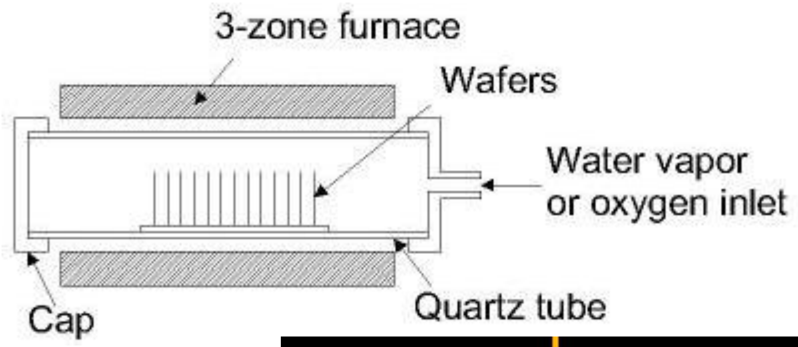
- In some cases, these methods can be considered bottom-up

https://www.youtube.com/watch?v=JJEILA8k6Qg https://www.youtube.com/watch?v=ljbESGs1XrM

Thermal oxidation

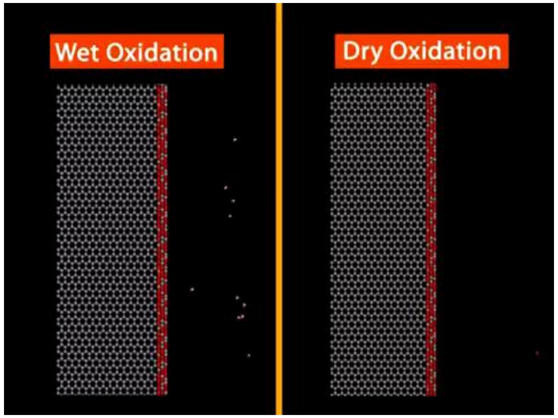
- Process to grow SiO_2 by oxidizing the Si substrate

- High temperature, oxygen atmosphere
- Reaction happens on the surface, but diffusion drives layer growth
  - Temperature and time are key parameters to determine final thickness



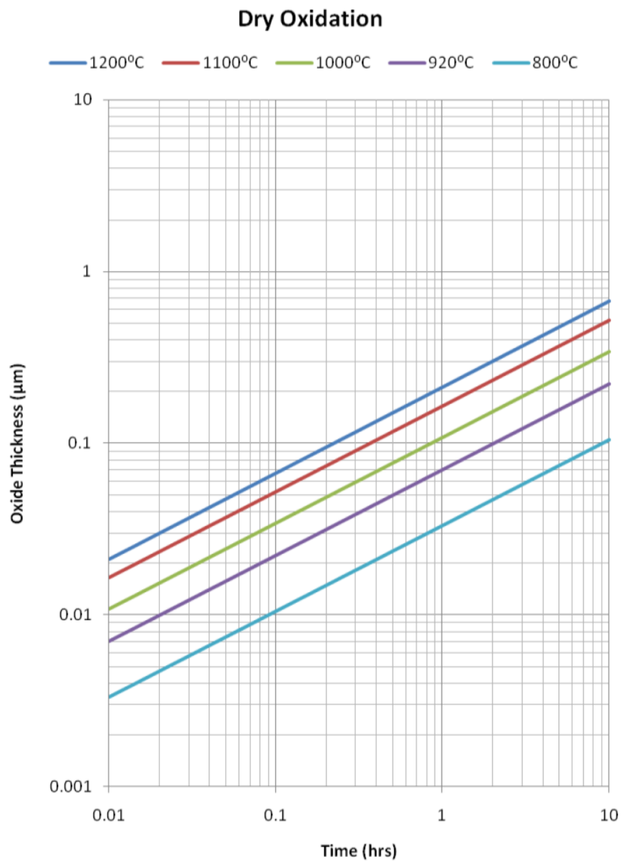
- Types of oxidation
  - Dry – Oxygen gas in the chamber
  - Wet – Water vapor in the chamber

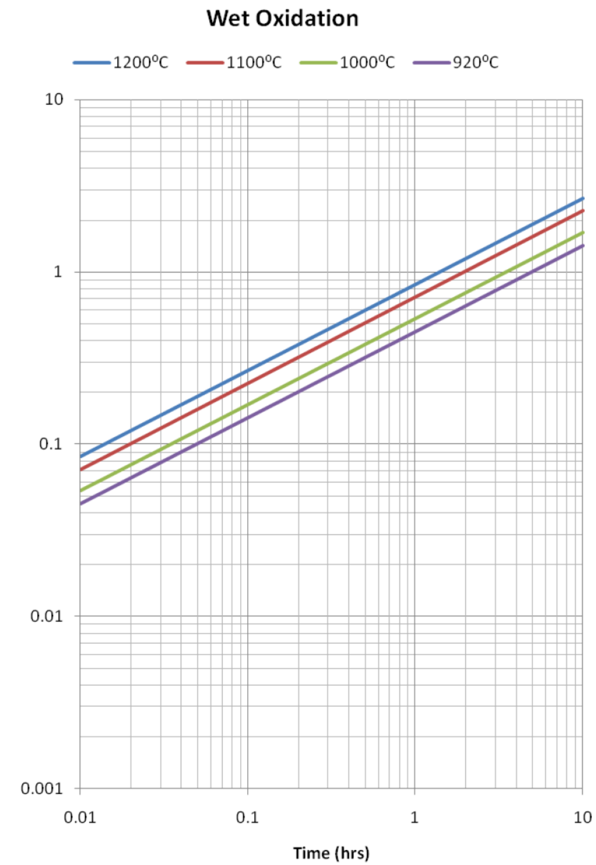
- Wet oxidation is faster
- Dry oxidation yields higher quality oxide



Thermal oxidation – Process parameters

- Temperature
- Time
- Si surface exposed
- Type of oxidation
- Si doping



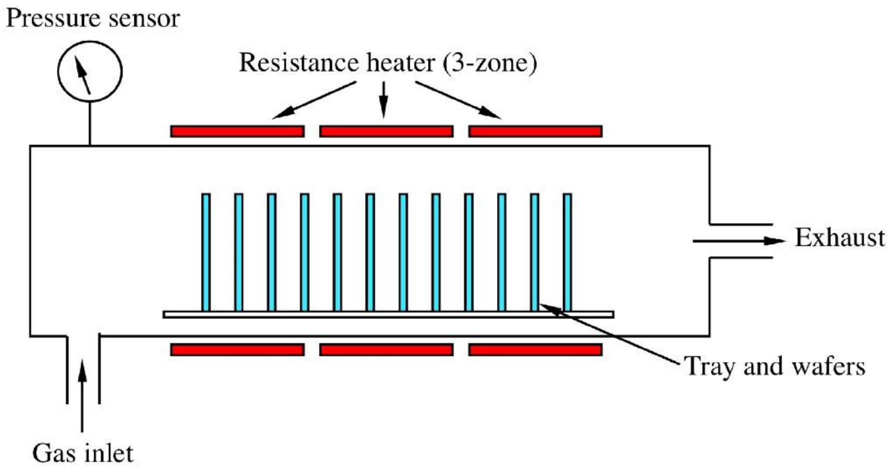


- Diffusion of OH^- into Si is faster than O^{2-}
- Wet – for thick layers; Dry – for thin, high quality layers
- Oxidation happens at RT – saturates at 2-3 nm approx. – **Native oxide**

Chemical Vapor Deposition (CVD)

- Deposition of material on the substrate upon:
  - Chemical reaction between gases
  - Chemical reaction between reagents and surface
- CVD is a very conformal technique (material also deposits on vertical walls)

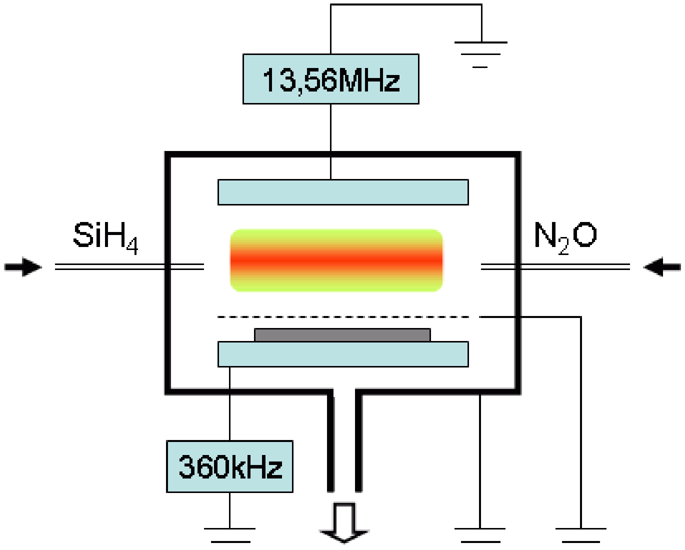
- **LPCVD – Low Pressure CVD**
  - Classical technique
  - Reaction happens at high T and low P



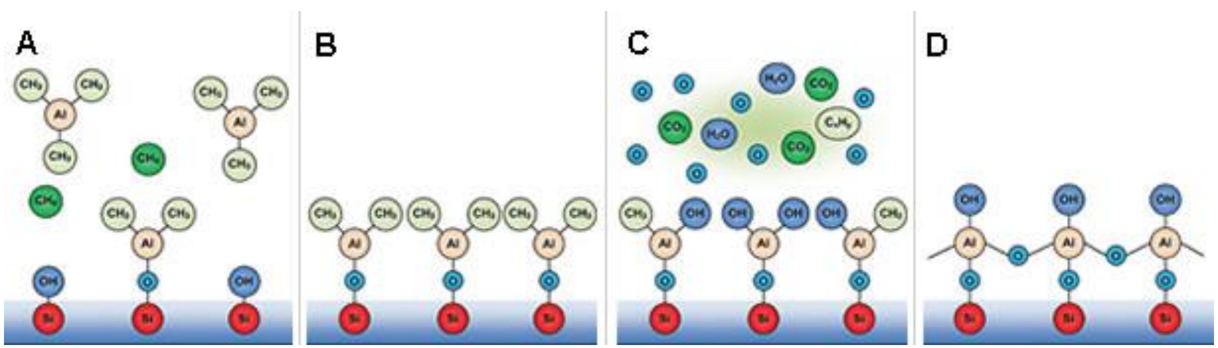
- Silicon Nitride
  - Gases: NH_3 and $SiCl_2H_2$
  - T and gas flow ratio determine
  - Stoichiometry, mechanical and optical properties of the material

Chemical Vapor Deposition (CVD)

- **PECVD – Plasma enhanced CVD**
  - Relatively modern technique
  - For substrates that cannot withstand high T
  - Reaction is facilitated by a plasma creation
  - Silicon oxide (SiH_4+NO_2)
  - Silicon nitride (SiH_4+NH_3)



- **ALD – Atomic layer deposition**
  - Self limiting chemical reaction on the surface
  - Enables grow layer-by-layer (atomic level)
  - Al_2O_3



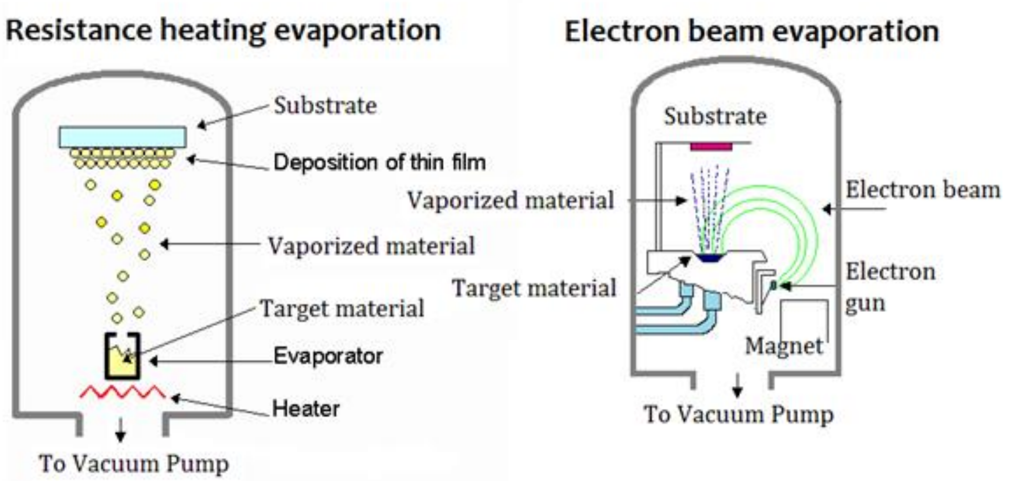
TMA chemisorption

Oxygen plasma

Physical Vapor Deposition (PVD)

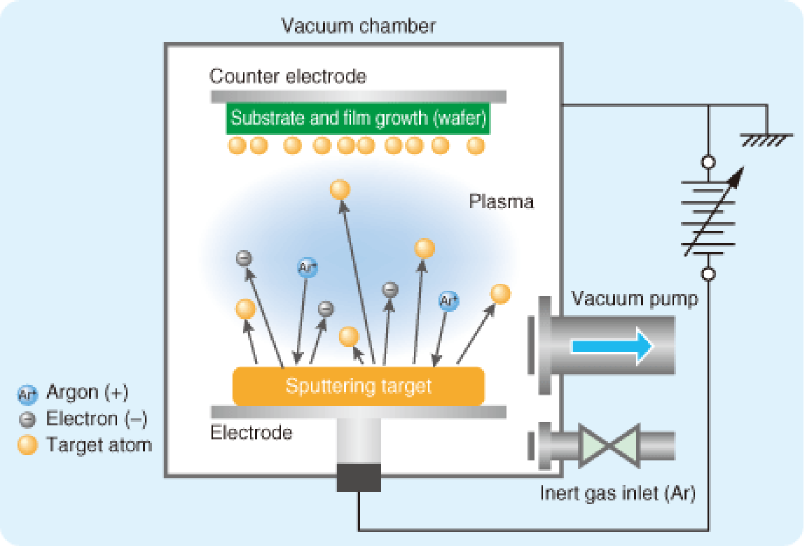
- Material is vaporized from source and solidifies on the substrate
  - Pure physical process in most cases (no chemical reaction)
  - Normally used for metals
- Directional deposition

- **Evaporation**
  - Very low pressure kept **during process** ($< 5 \cdot 10^{-6}$ mbar)
  - Material source is brought beyond its boiling point
  - Resistance or e-beam heating
  - Several wafers can be processed at a time, for which rotation of the wafers



Physical Vapor Deposition (PVD)

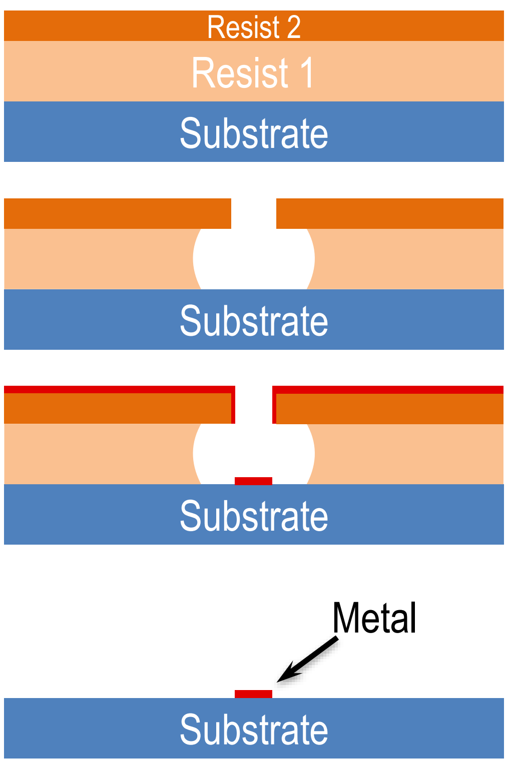
- **Sputtering**
  - Very low **base pressure**
  - Ar is inserted in chamber and plasma started
  - Atoms from material source are extracted via collisions of accelerated ions
  - During process $\mathrm{P} \sim 10^{-3}\ \mathrm{mbar}$
    - Collisions between different atoms make the deposition more conformal

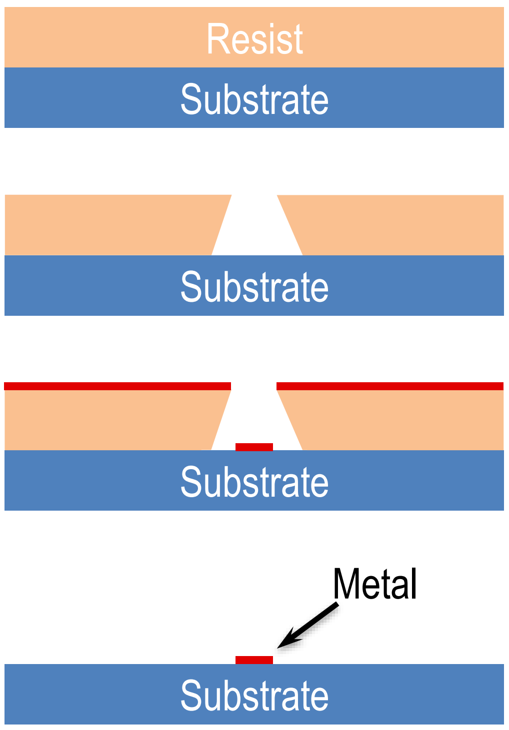


- **Reactive sputtering**
  - Ar and a reactive gas (e.g. Nitrogen) are inserted in the chamber
  - On the material source surface, reactive gas reacts thanks to the plasma energy
  - The newly generated material travels to the substrate

Lift-off process

- Technique to pattern material without etching
  - In essence, we "lift-off" what we do not want
- Directionality of deposition is critical



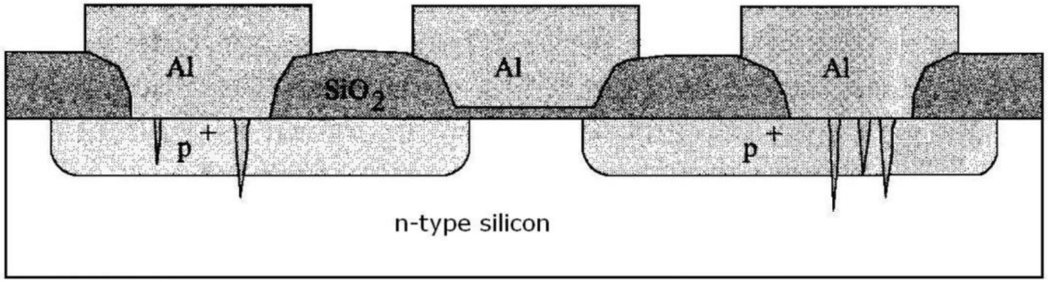


Main issues

- Thermal budget of the process
  - Metal diffusion
  - Metal desorption
- Stress in thin films
  - Adhesion improvement
  - Flat mechanical structures
- Contamination
- Continuous layers
- Proper metal contact
- Lift-off

Main issues

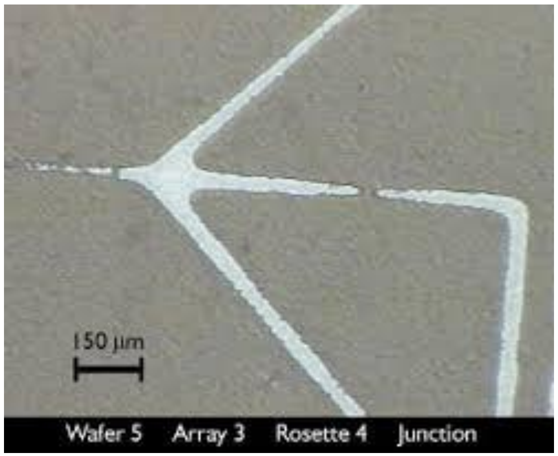
- Thermal budget of the process
  - Metal diffusion
    - Al spikes into Si
      - Oxide
      - Al-Si alloy
    - Au into Si
      - Oxide
      - Cr as adhesion/diffusion barrier
    - Au into Ti
      - Ni or Pt in between

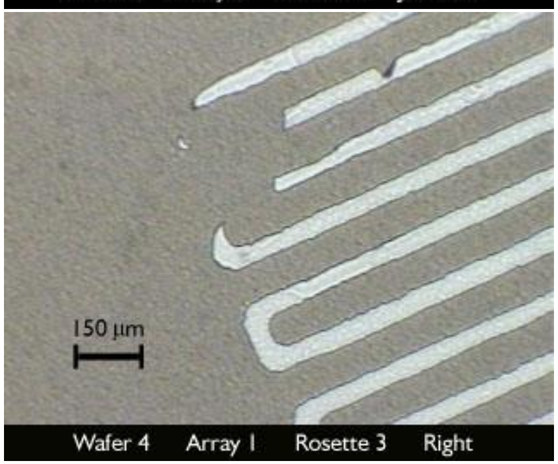


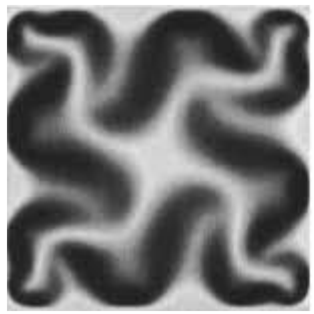
  - Metal desorption
    - Main problem for cros-contamination of wafers
  - Polymer stability

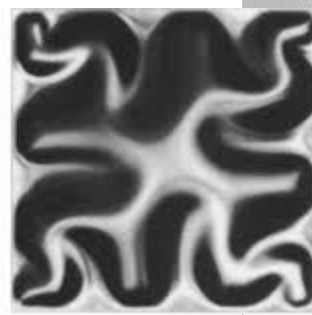
Main issues

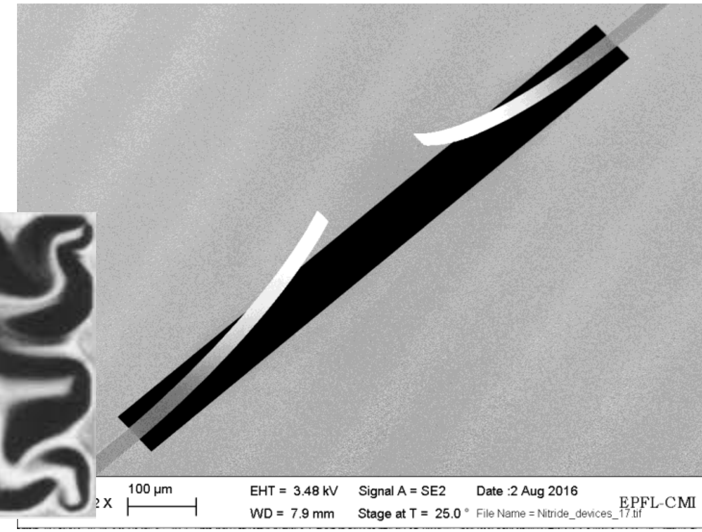
- Stress in thin films
  - Adhesion improvement
  - Flat mechanical structures

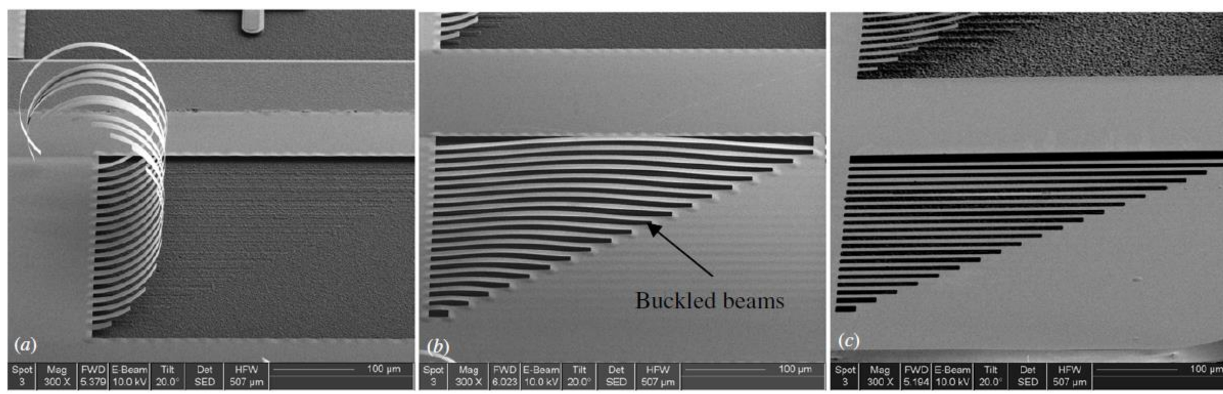








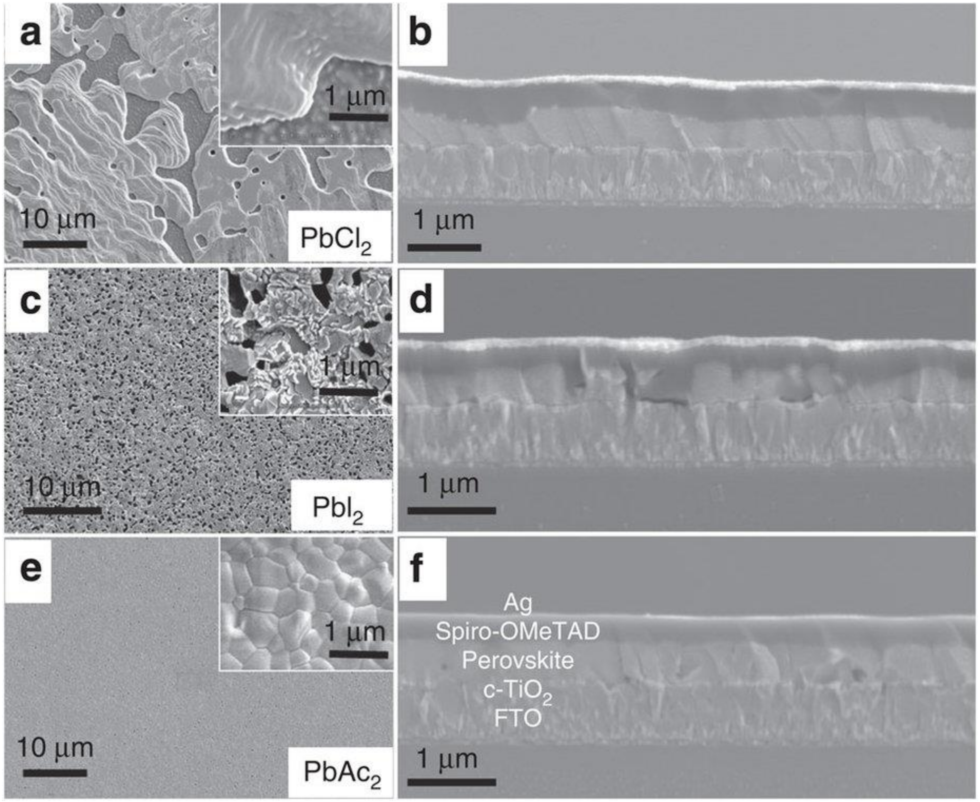




Main issues

- Contamination
  - Cross-contamination of other wafers
    - Previously deposited material can come on your wafer
    - Material that desorps can also come on a later wafer
  - Purity of the material
    - E.g. Josephson junctions

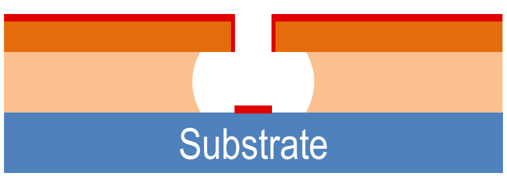
- Continuous layers
  - Continuity
  - Pinholes
    - Deposit thicker layer
    - Pay attention to substrate, T

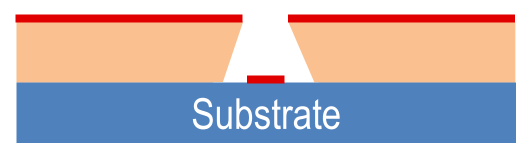


Main issues

- Proper metal contact
  - Clean surface
  - Good work-function matching (e.g. Si+Ti+Al)
  - Annealing to form alloy (e.g. Al+Si)

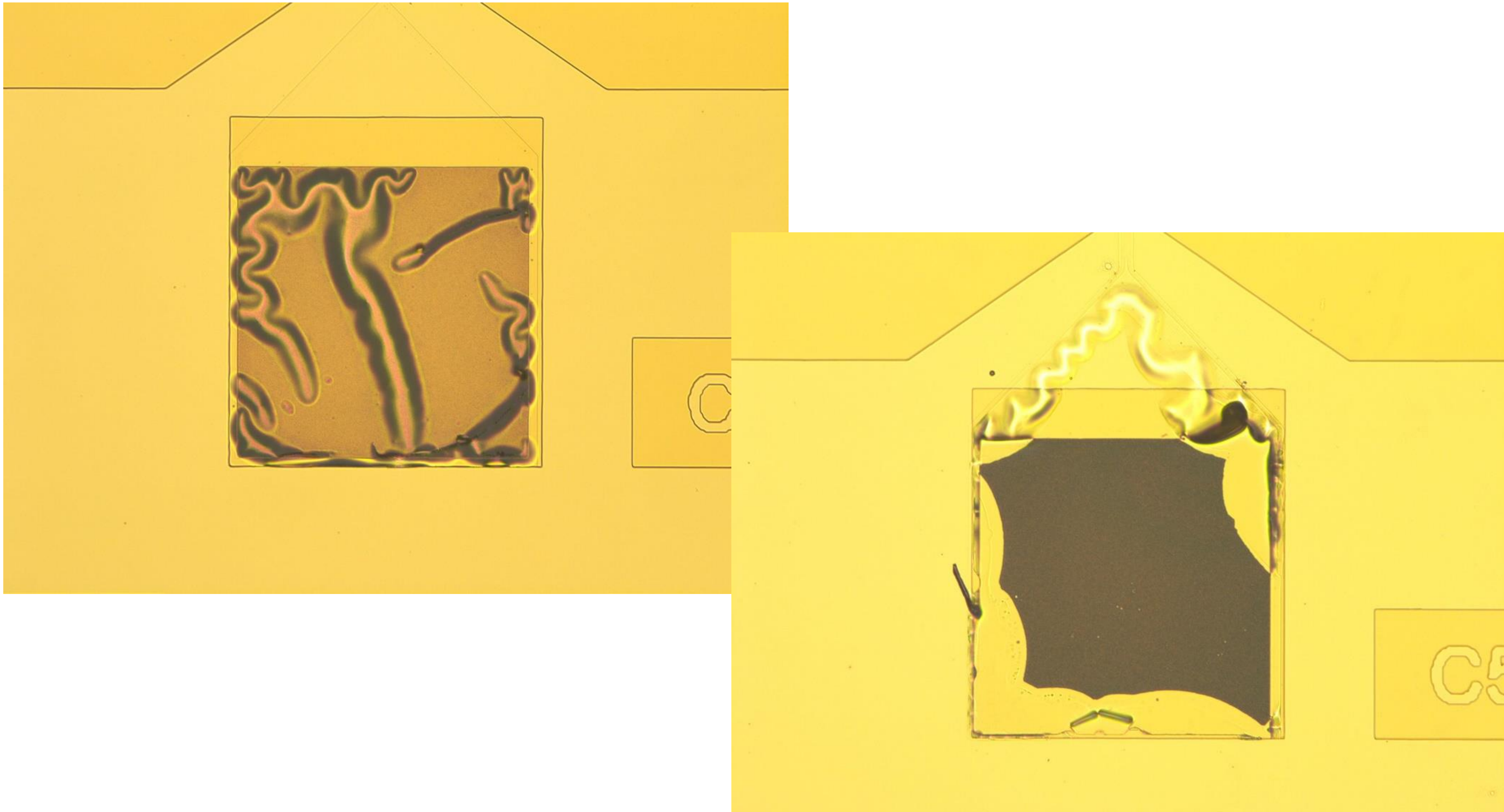
- Lift-off
  - “Does not work”
    - Ultrasounds, warm remover, remover with low vapor pressure
  - Works so-so
    - Adhesion layer
    - Low pressure & Large distance to source
    - Extra development
    - Oxygen plasma descum before deposition





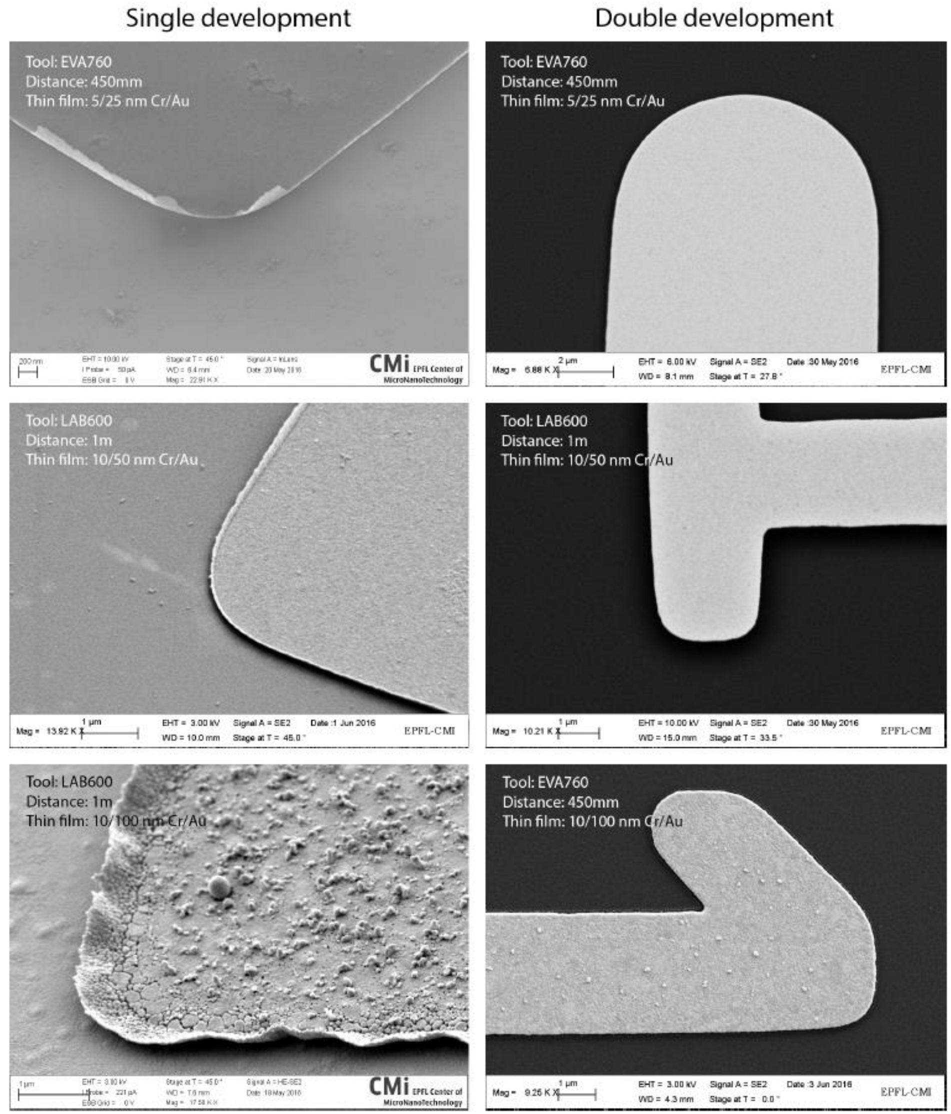
Main issues – Lift-off

- Adhesion layer



Main issues – Lift-off

- Distance to source
- Extra development



Summary table

Deposition

- Wet&Dry oxidation of Si
- Chemical processes
- Physical processes
- Lift-off – pattern without etching

Implantation

- Dope Si – transistors, etc.
- Generate new substrates – SOI
- Ion energy and dose
- Annealing is critical for “nano”

TOP-DOWN

Etching

Lithography

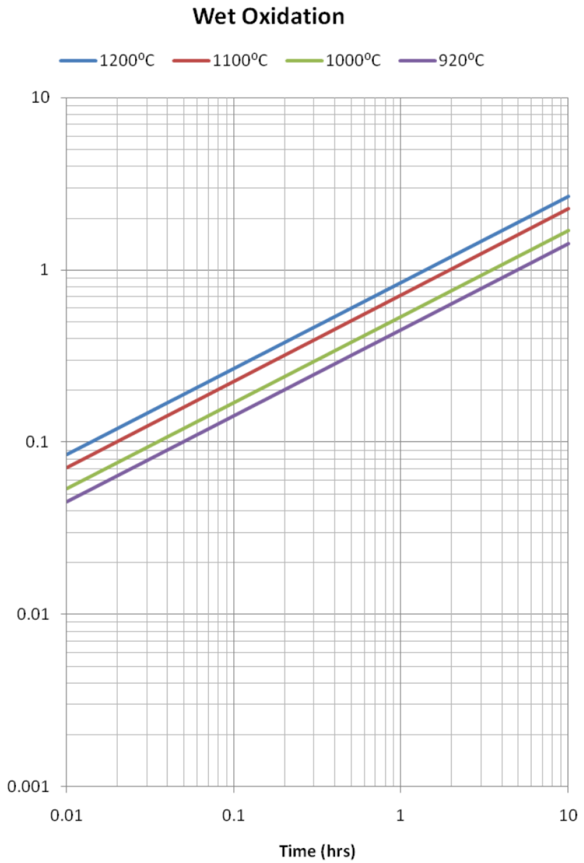
- Method to “draw” on the wafer
- Optical, EBL, NIL, …
- Best option depends on design, requirements and $$$

Which type of oxidation should we use to grow 1 micron of oxide?

A. Wet
B. Dry

How long would that take if done at 1100ºC?

A. 30 minutes
B. 45 minutes
C. 1 hour
D. 90 minutes
E. 2 hours
F. 4 hours



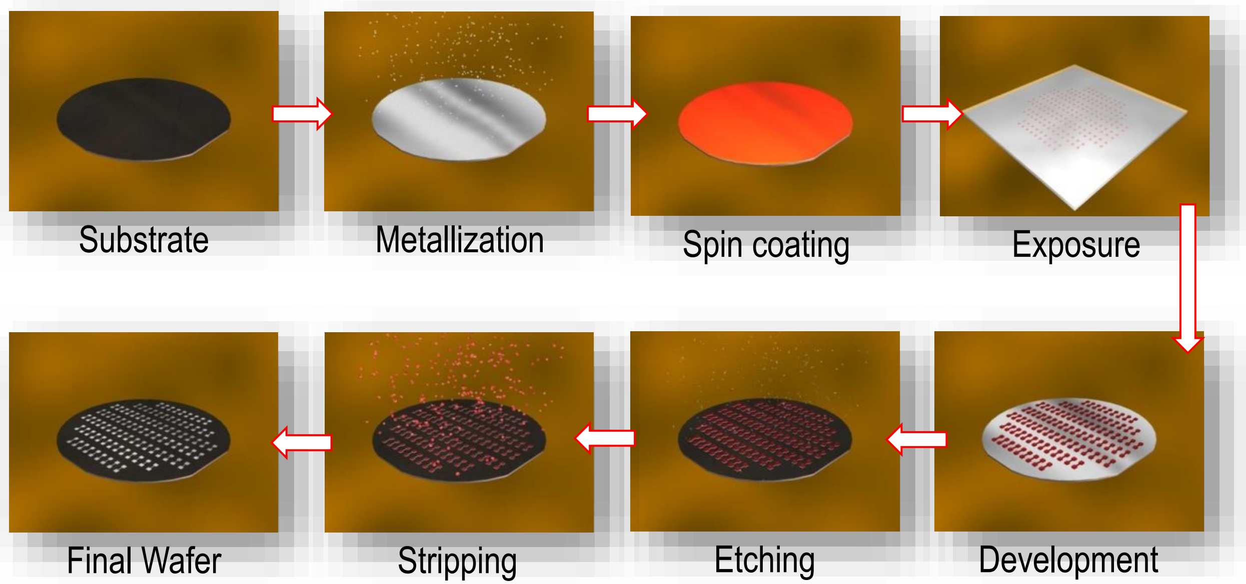
In order to make a metal line using lift-off, we should use...

A. Evaporation
B. LPCVD
C. Sputtering
D. Oxidation

Etching

Etching

- Process to remove select materials from the wafer surface



- Types
  - Wet etching
  - Dry etching
- Definitions:
  - Etch rate: rate at which the material is removed from the wafer (e.g. nm/min)
  - Selectivity: ratio between the etch rates for two different materials (dimensionless)

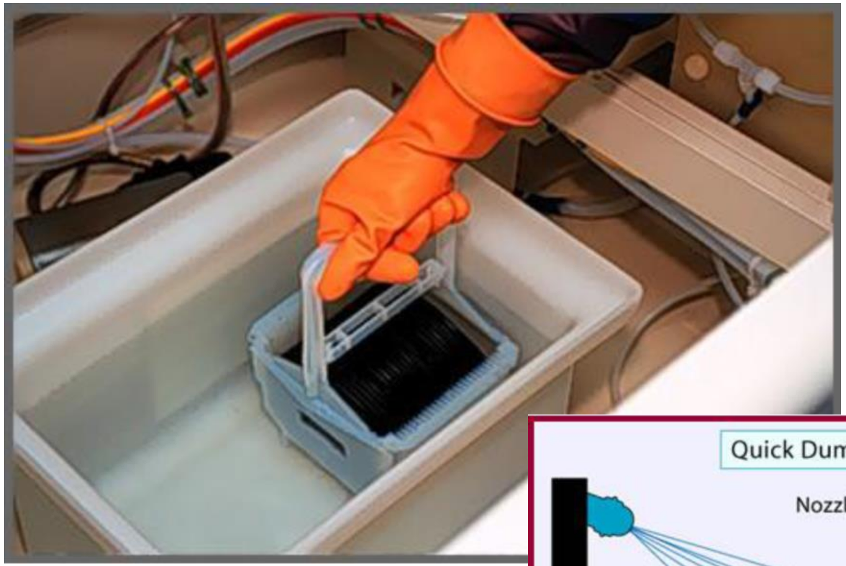
https://www.youtube.com/watch?v=UKf0offCyw0 https://www.youtube.com/watch?v=D9r0ZBNIq48

Wet Etching

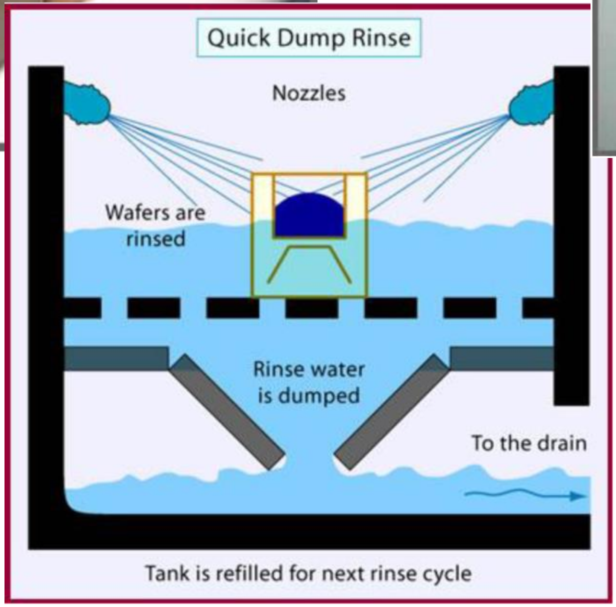
- Material is removed through a chemical reaction with a liquid etchant
  - Highly selective etchings
  - Strongly depend on Temperature

- Caution! Hazardous chemicals:
  - Work in a wet bench with an exhaust
  - Wear protective garment

Wet Etching - Steps



Etching



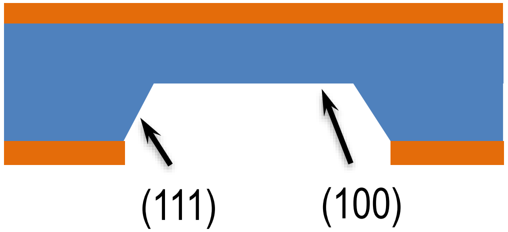
Rinsing

Drying

Examples

- **SiO_2** – HF – Isotropic etching

- **Si** – KOH, TMAH – Anisotropic etching (etch rate depends on crystal plane)



- **Polycrystalline Silicon** – KOH, TMAH – Isotropic etching

Dry etching

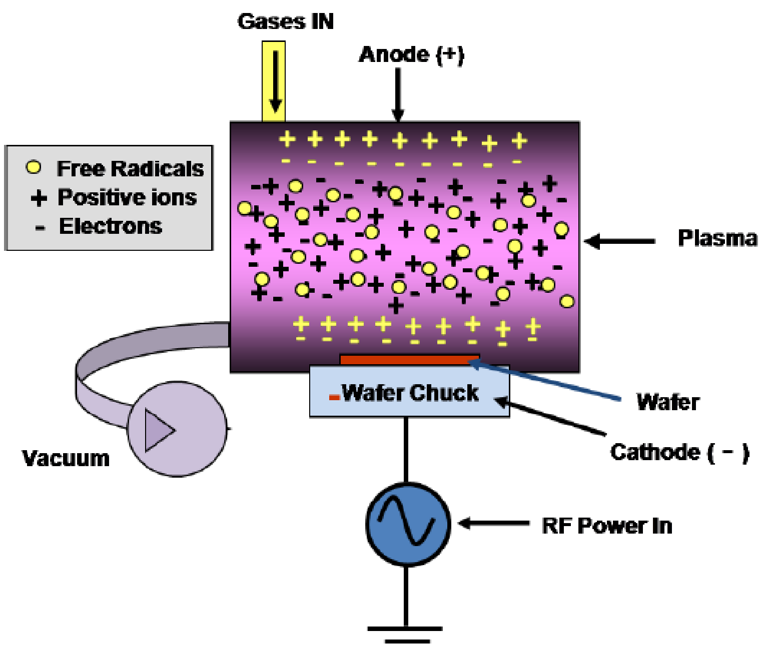
- Wafers exposed to gaseous etchant suspended in RF-energized plasma
  - Chamber is filled with a mixture of electrons, ions and radicals

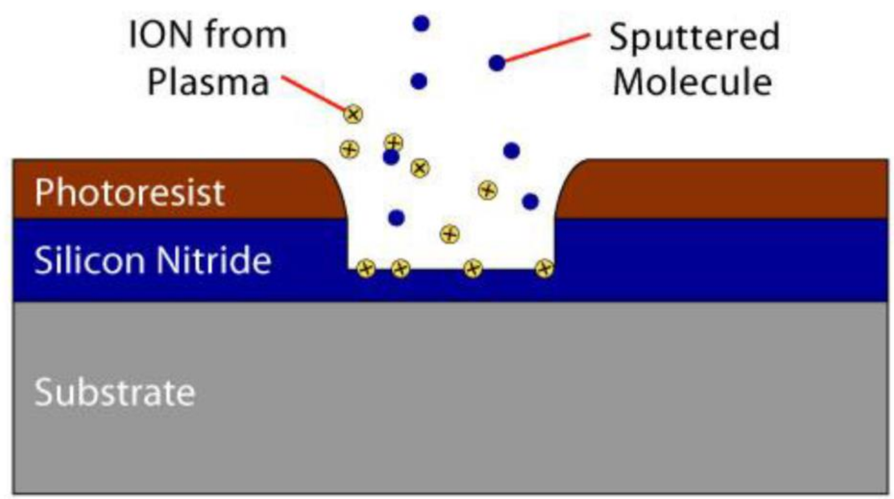
- Compared to wet etching
  - Process parameters' space is much larger and with a better control
  - By tuning those parameters, we can control etching profile: e.g. anisotropy

- Tuning parameters allows us to move between 2 regimes:
  - Chemical dry etching **Reactive Ion Etching (RIE)**
  - Physical dry etching

Physical dry etching (IBE – Ion Beam Etching)

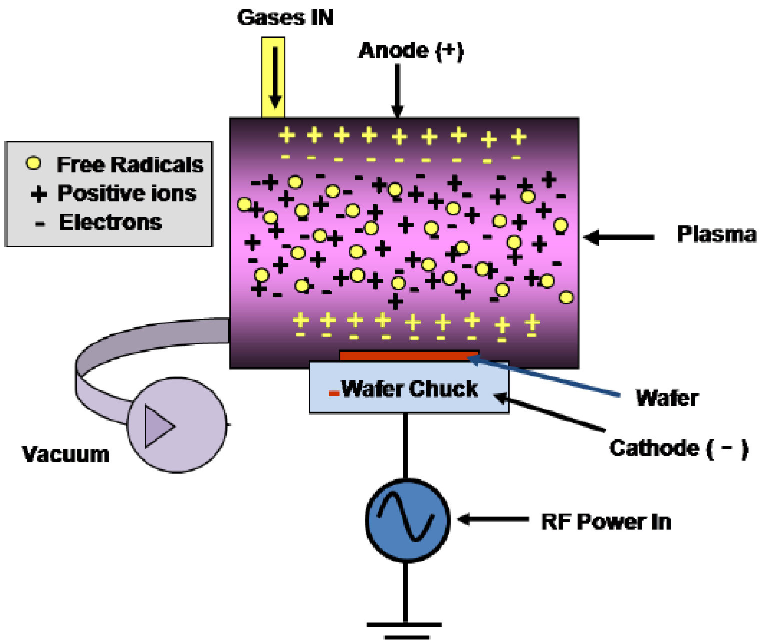
- Ions from plasma are accelerated towards the wafer
- Highly energetic impact causes material to sputter away
  - Same principle as we saw during sputtering deposition
- Selectivity between different materials is given by hardness

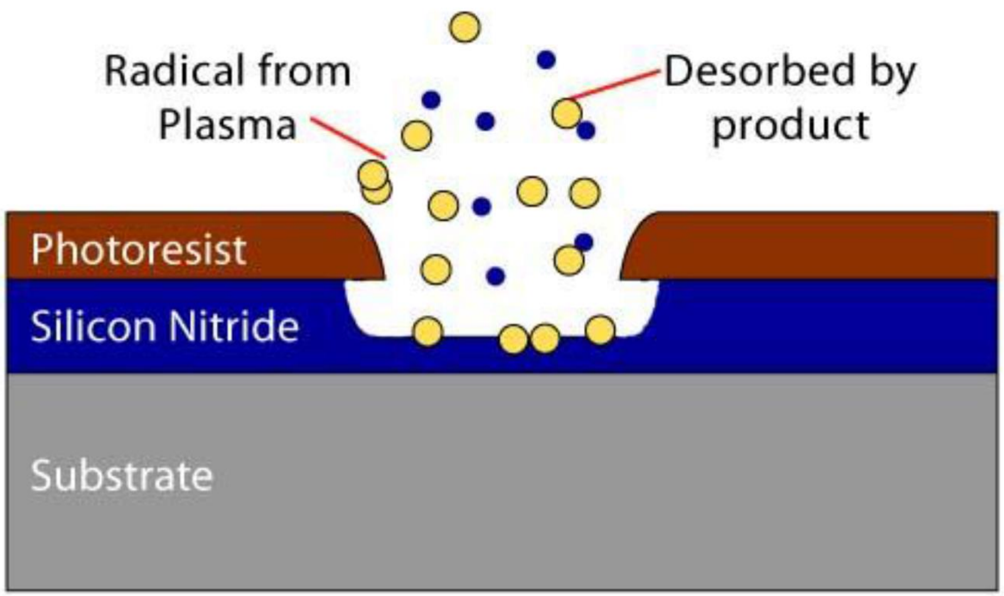




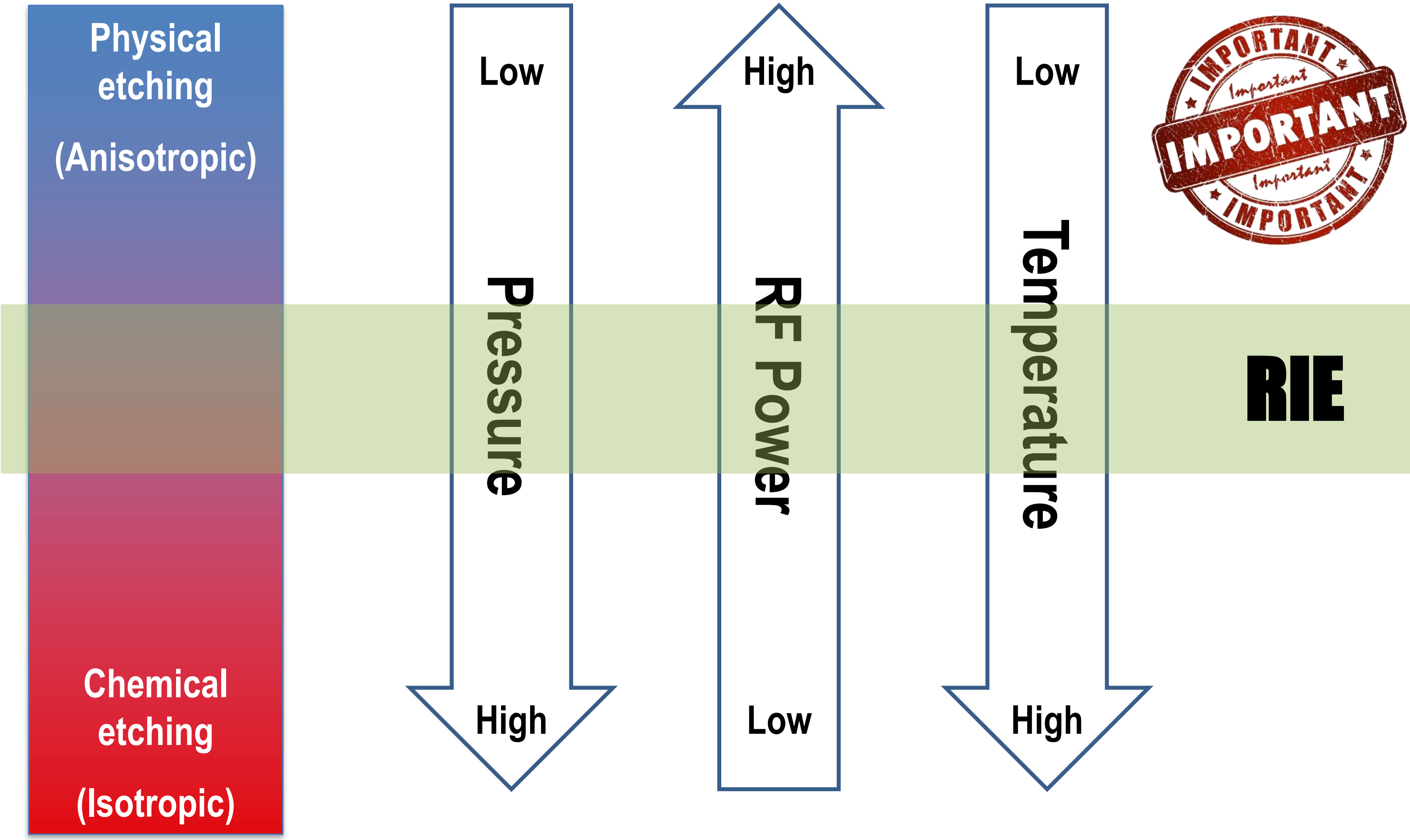
Chemical dry etching

- Free radicals from plasma are adsorbed and a chemical reaction occurs
- The products of this chemical reaction are desorbed from the wafer
  - Similar to what we discussed during wet etching
- Selectivity is determined by the chemical reactivity of each material



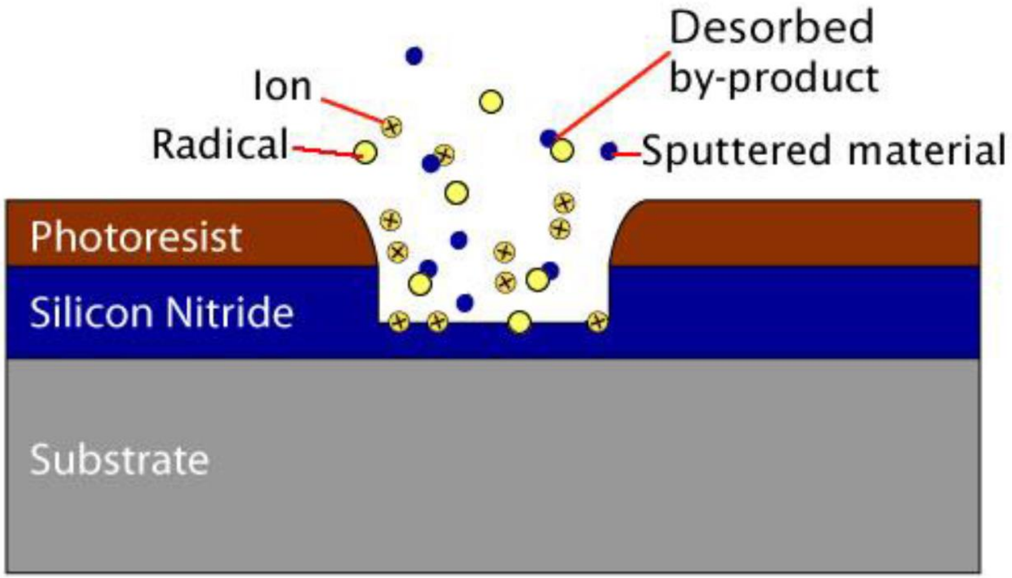


Basic process parameters



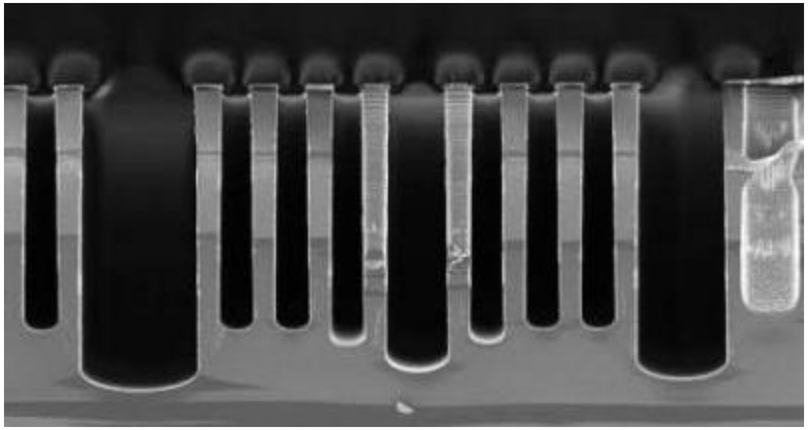
Reactive Ion Etching (RIE)

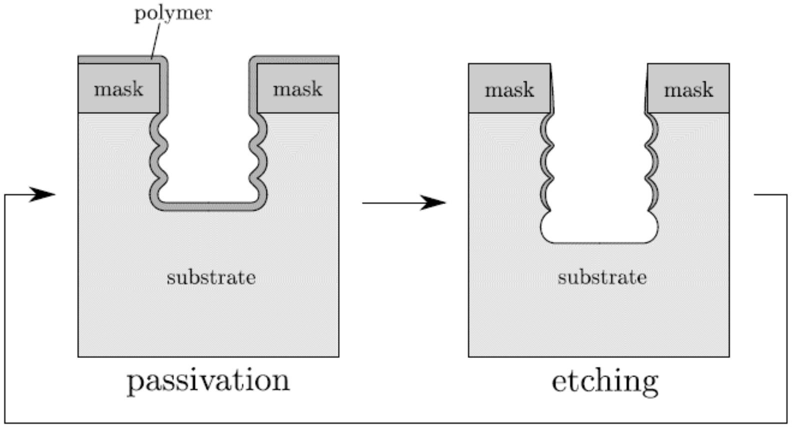
- Makes use of both ions and radicals to have a combination of physical and chemical etching
- In addition, there are some chemical reactions in the surface that are enabled by the ionic impact
  - *The whole is greater than the sum of its parts*
- Most used etching technique in micro- and nano-fabrication



Inhibitor gases

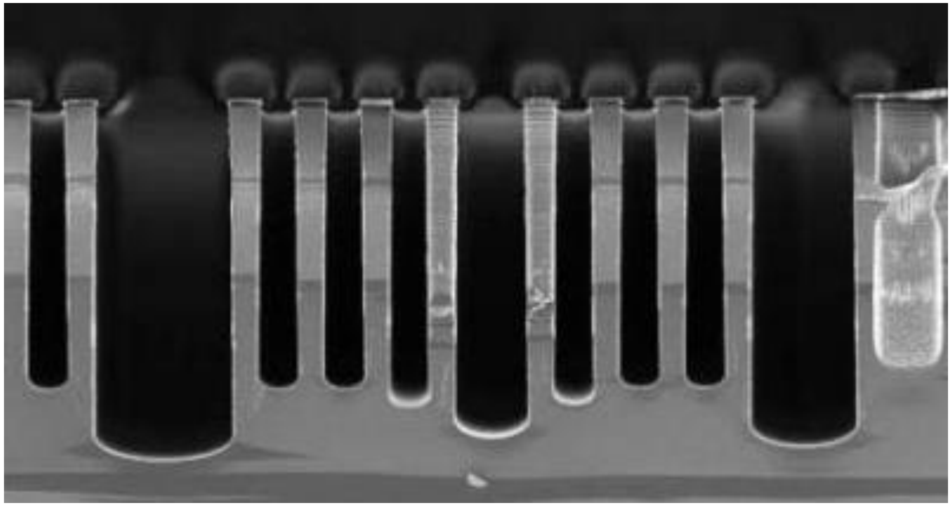
- It is possible to insert in the chamber gases that instead of etching generate a passivating polymer
- This polymer will cover both vertical and horizontal walls, but will be only removed on the horizontal walls, facilitated by ions energy
- Example: **Bosch® process**
  - SF_6 and c-C_4F_8
  - Etching and passivation





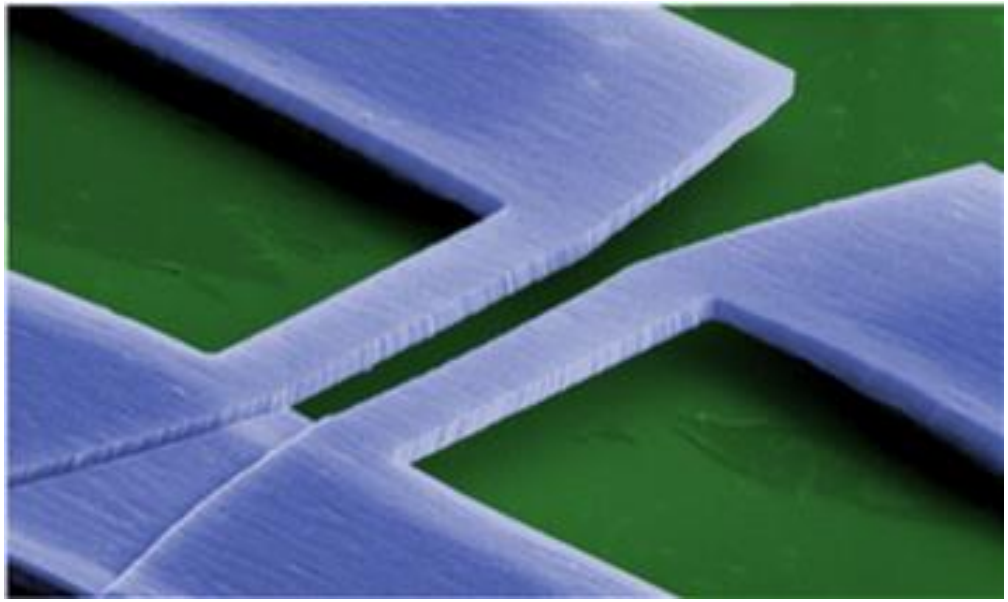
Effects to pay attention

- ARDE – Aspect ratio dependent etching
- Uniformity across the wafer – SoA ~5%
- Load dependence – Etch rate depends on the % of the wafer to be etched



Particular challenges for Nano

- Reproducibility
- Lateral roughness
- Polymer residues

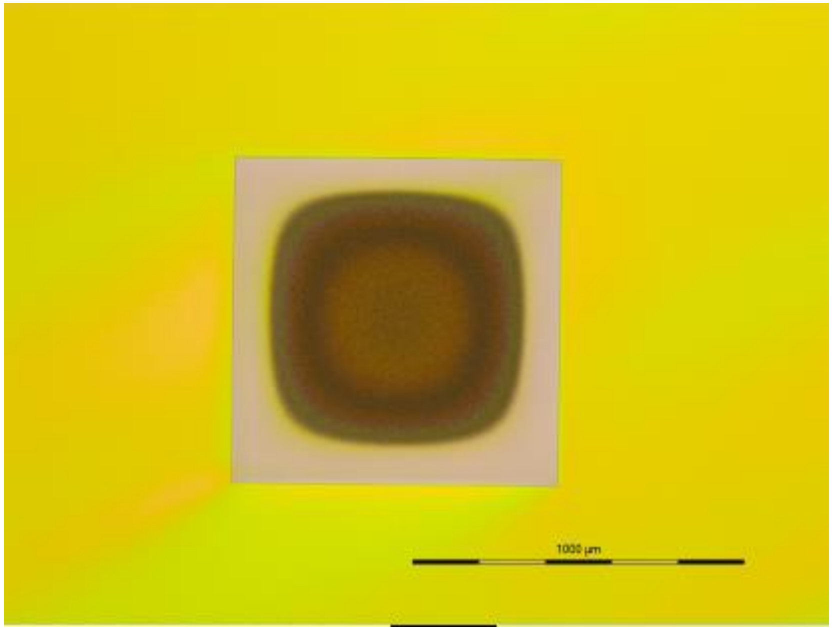


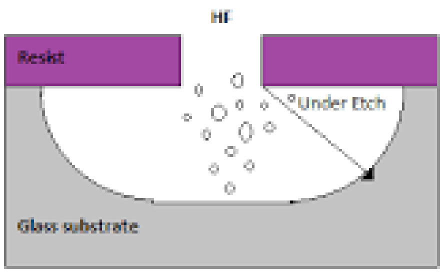
Main issues

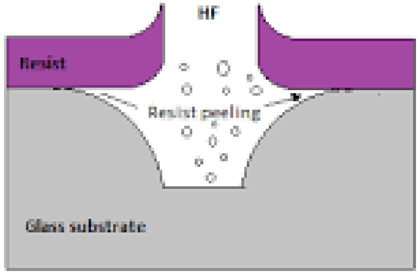
- Resist
  - Delamination – Wet etching
  - Burnt resist – Dry etching
- "Grass"-like result
- Over-etching
  - Lateral
- Fences
- Polymer residues

Main issues

- Resist
  - Delamination – Wet etching
    - (Hard)-Bake of resist
    - Special attention to HF and –OH solutions
  - Burnt resist – Dry etching
    - Improved thermal contact
    - Oxygen plasma to remove first layer

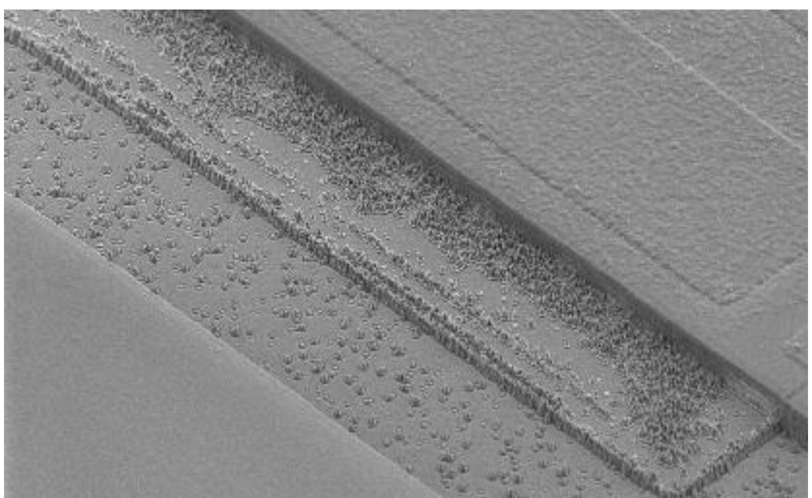


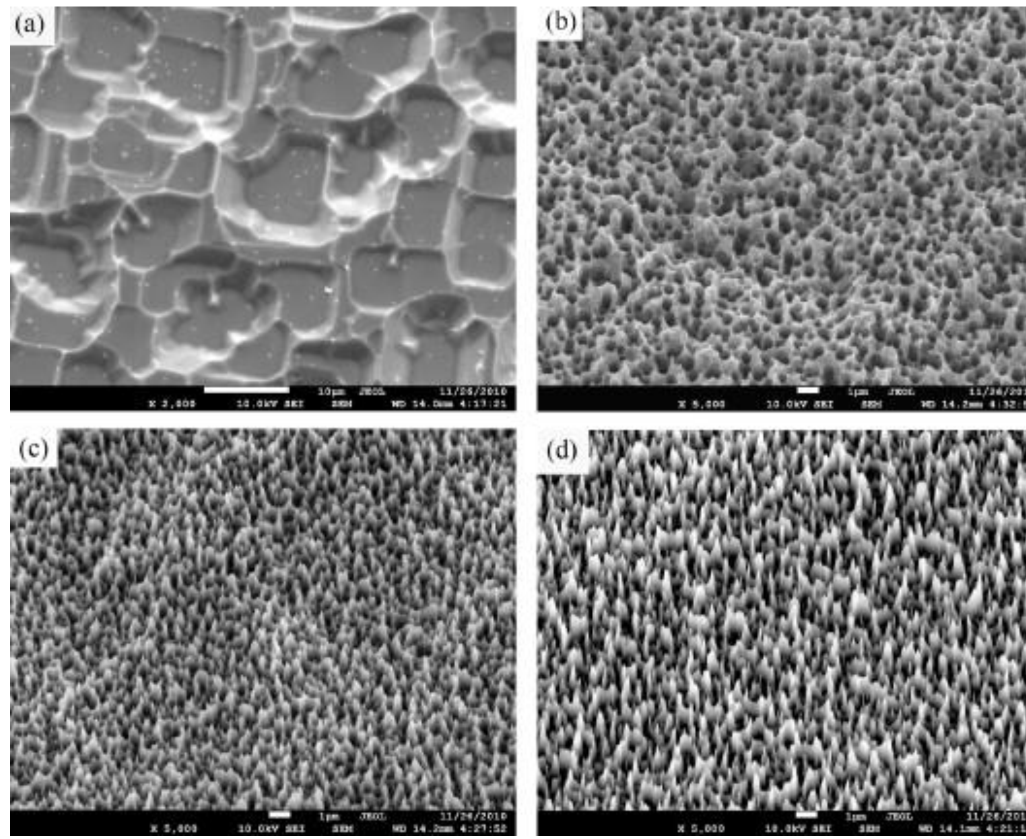




Main issues

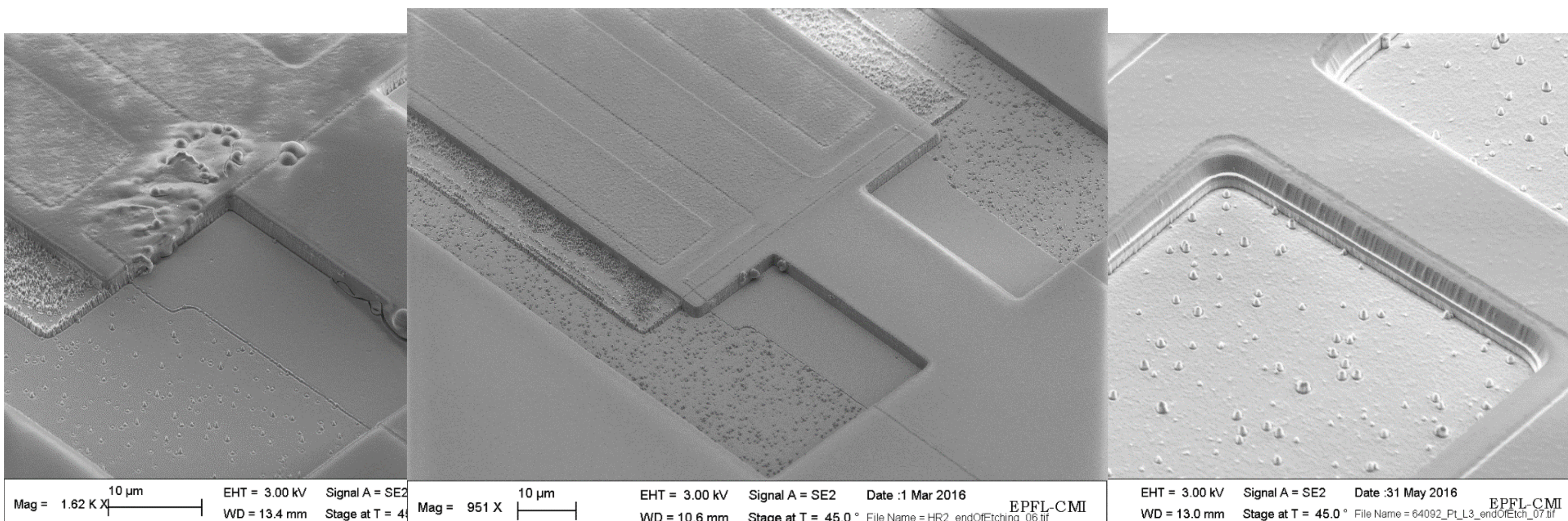
- "Grass"-like result
  - Huge selectivity difference
  - Balance between etching and passivation gases





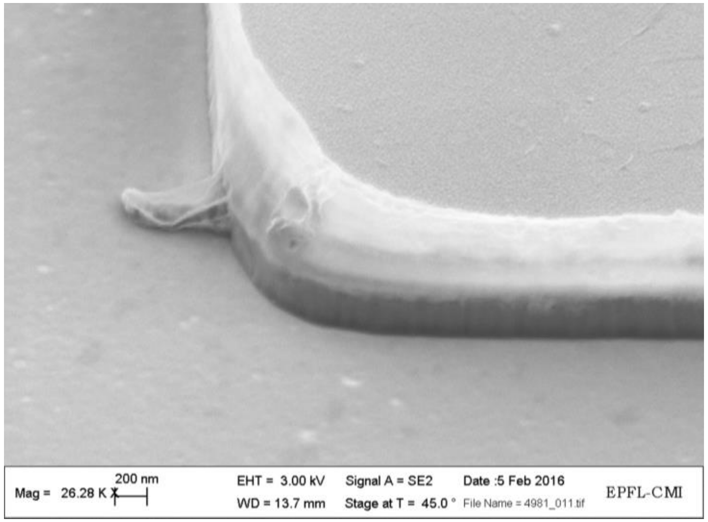
Main issues

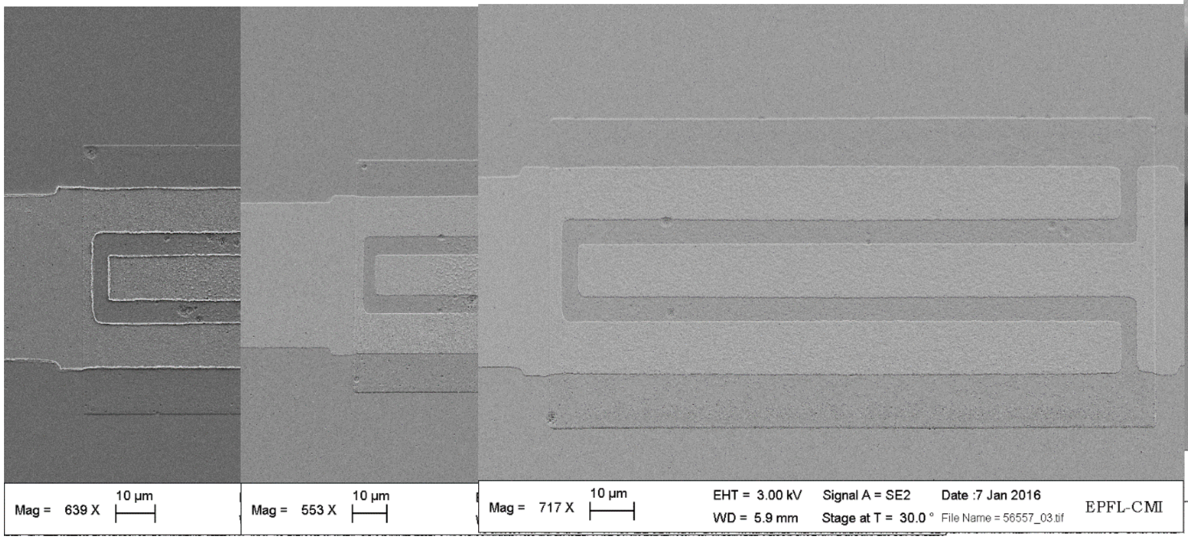
- Over-etching
  - Vertical
    - Always try to get safety margins
    - Etch half of the layer-to-be-etched to characterize the etch-rate
  - Lateral
    - In some cases, etching can continue after wafer is out of the chamber
    - E.g. Aluminum etching with Chlorine chemistry

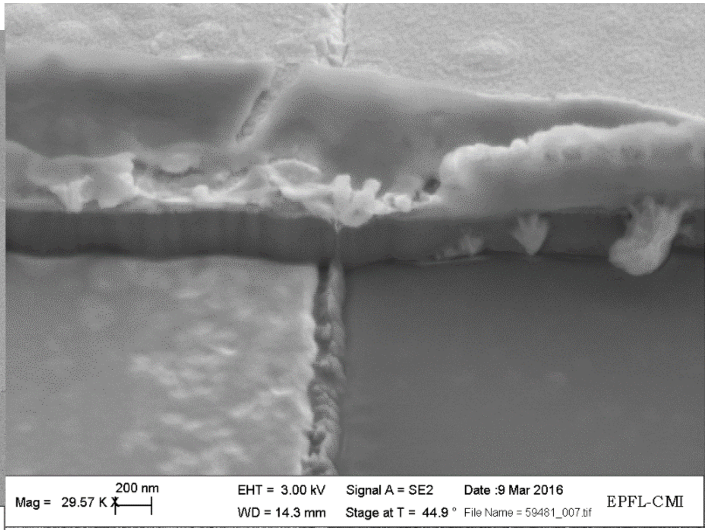


Main issues

- Fences
  - Redeposition of material on sidewalls
  - Specially important for IBE
    - Ultrasounds
    - Change etching machine/recipe







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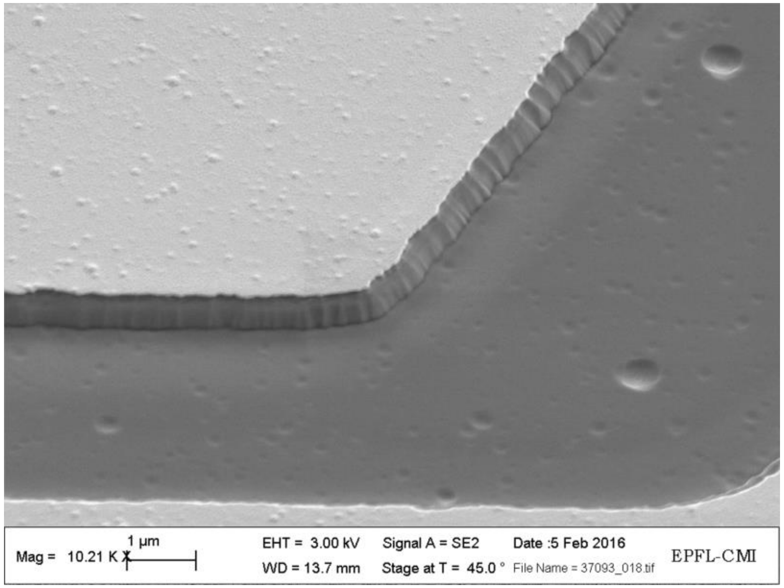
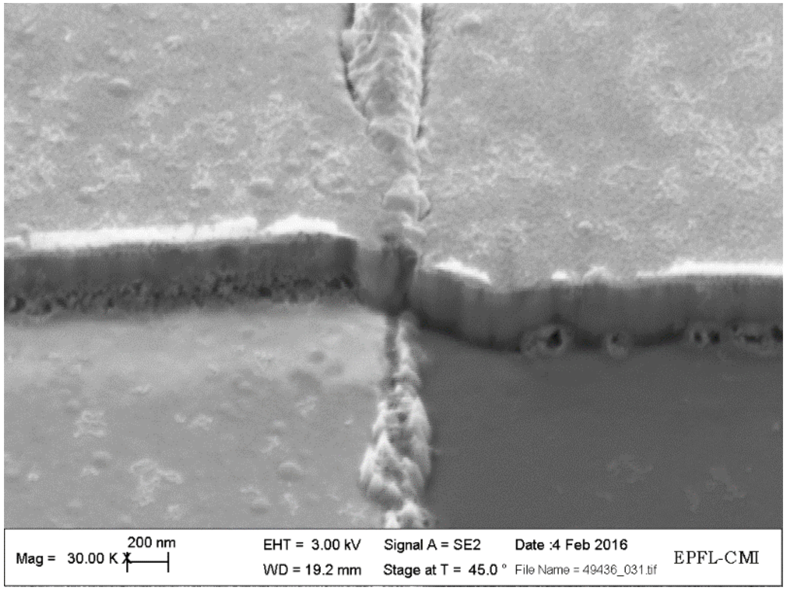
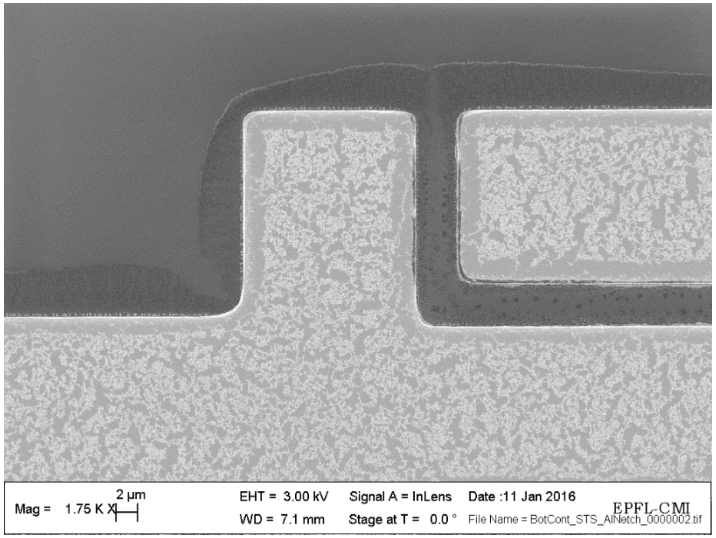
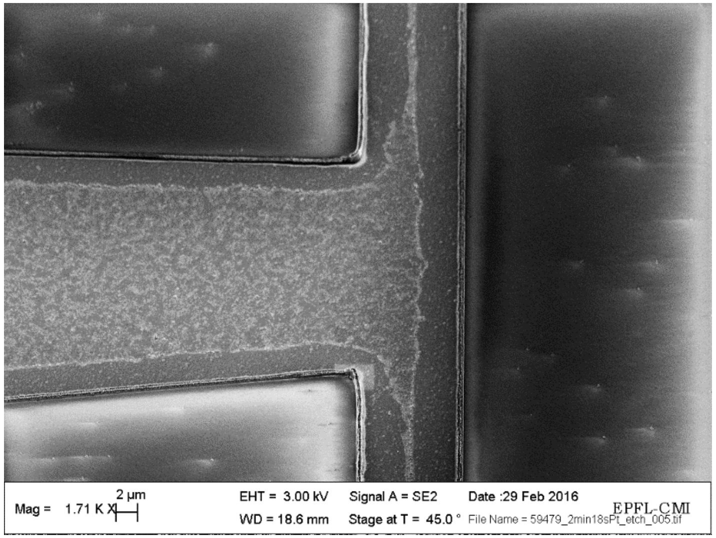




Main issues

- Polymer residues
  - After dry etching, some monolayers cannot be removed
    - This can affect subsequent steps
  - Specially important for noble metals
  - Deposit sacrificial layer in between resist and substrate e.g. SiO2





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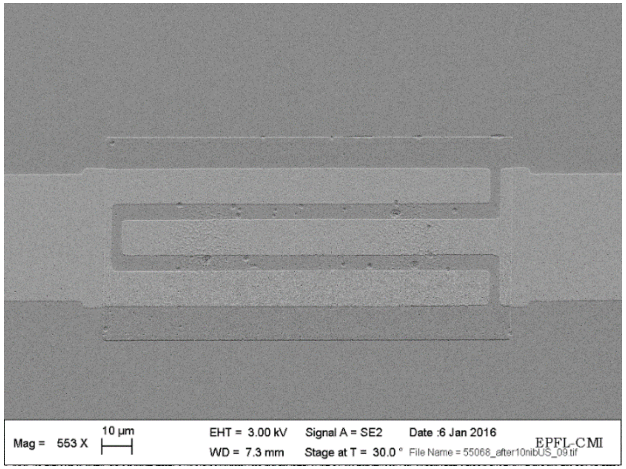

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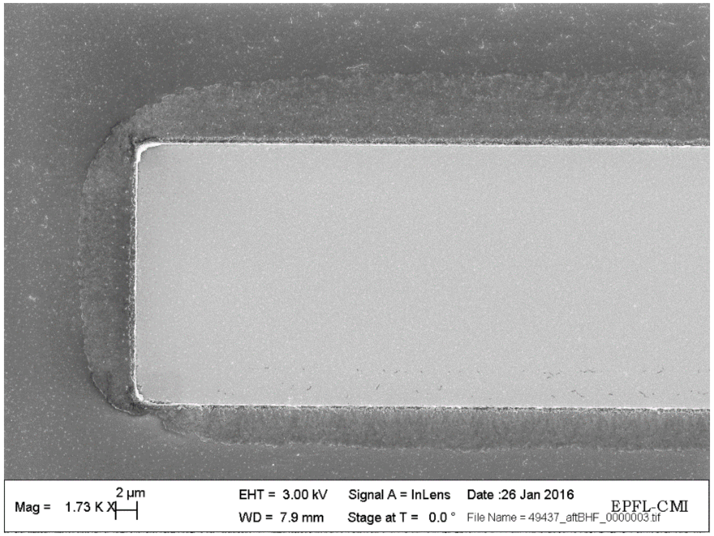
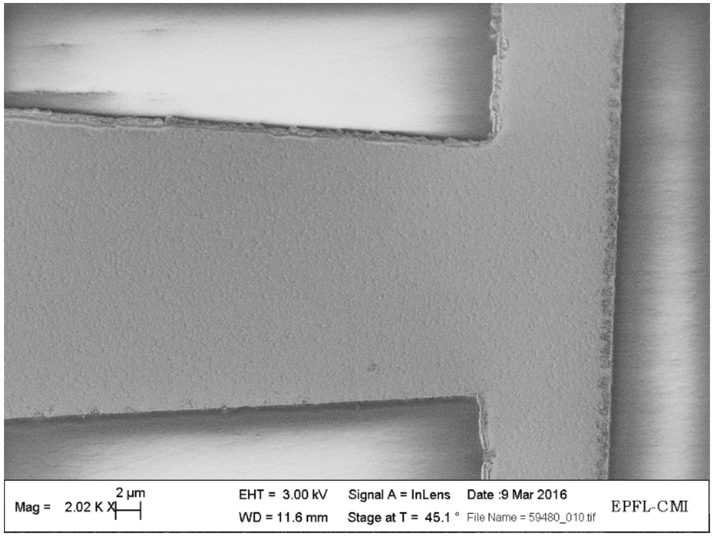




Summary table

TOP-DOWN

Deposition

- Wet&Dry oxidation of Si
- Chemical processes
- Physical processes
- Lift-off – pattern without etching

Implantation

- Dope Si – transistors, etc.
- Generate new substrates – SOI
- Ion energy and dose
- Annealing is critical for "nano"

Etching

- Wet etching – Purely chemical
- Dry etching – can be tuned between chemical and physical
- Issues – uniformity, reproducibility

Lithography

- Method to "draw" on the wafer
- Optical, EBL, NIL, …
- Best option depends on design, requirements and $$$

Is it possible to define vertical walls in Si using wet etching?

A. Yes
B. No

After a dry etch, the profile is not completely vertical. What can we change to improve it?

A. Increase pressure
B. Reduce T
C. Change the chemistry
D. Etch longer
E. Change the mask material

EPFL

Bottom-Up Methods

Chemical engineering

NPs	CNTs	NWs	2D

Summary table

Bottom-Up

NPs	CNTs	NWs	2D

Nanoparticle synthesis

The First Nanotechnologists

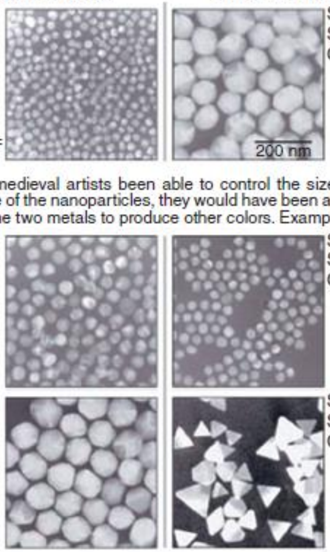
Ancient stained-glass makers knew that by putting varying, tiny amounts of gold and silver in the glass, they could preduce the red and yellow found in stained-glass windows. Similarly, today's scientists and engineers have found that it takes only small amounts of a nanoparticle, precisely placed, to change a material's physical properties.

Gold particles in glass | Silver particles in glass

Size*: 25 nm
Shape: sphere
Color reflected:

Size*: 100 nm
Shape: sphere
Color reflected:

100 nanometers = 0.0001 millimeter



Had medieval artists been able to control the size and shape of the nanoparticles, they would have been able to use the two metals to produce other colors. Examples:

Size*: 50 nm
Shape: sphere
Color reflected:

Size*: 40 nm
Shape: sphere
Color reflected:

Size*: 100 nm
Shape: sphere
Color reflected:

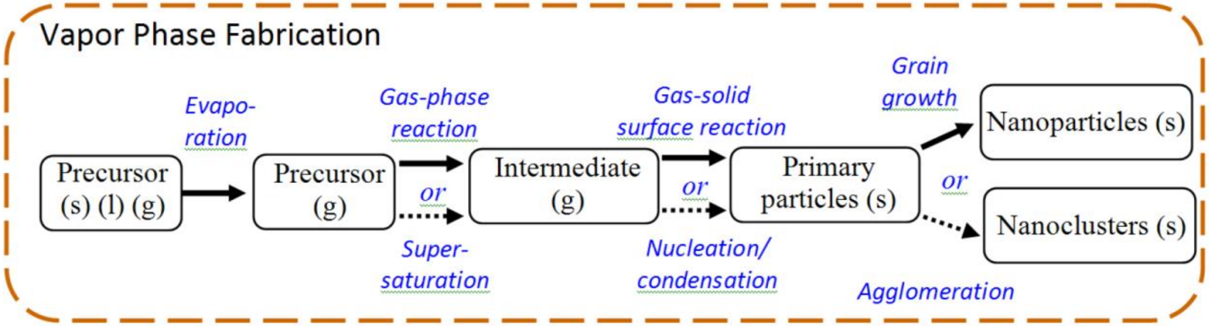
Size*: 100 nm
Shape: sphere
Color reflected:

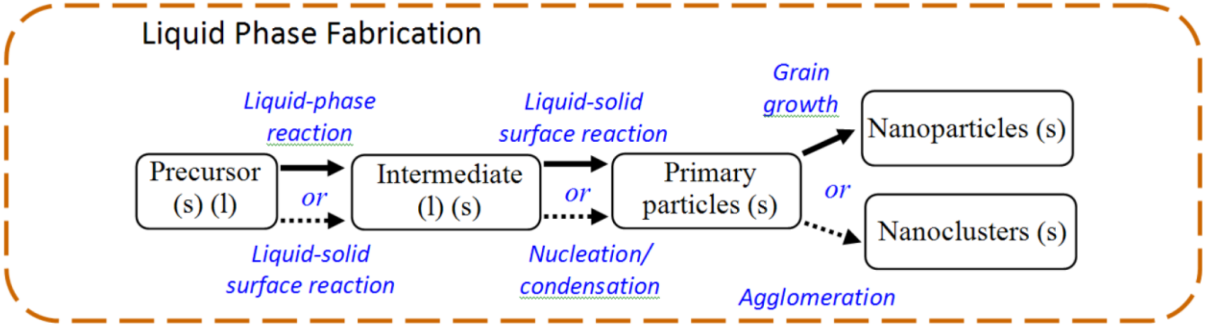
Source: Dr. Chad A. Mirkin, Institute of Nanotechnology, Northwestern University

*Approximate

Nanoparticle synthesis

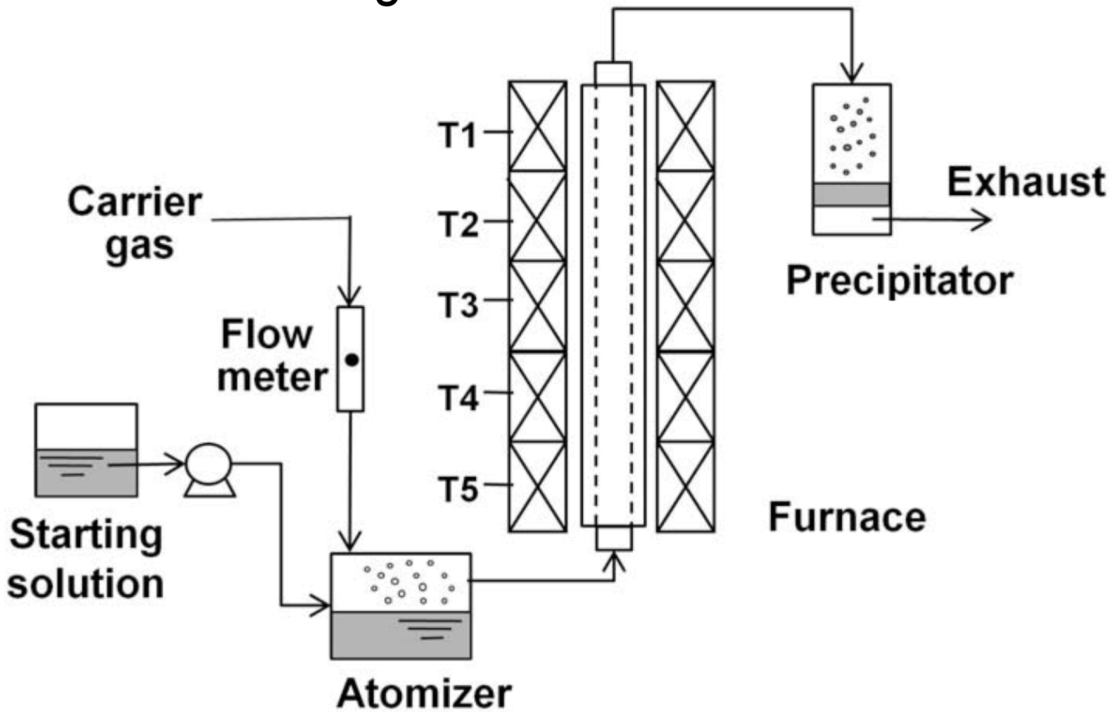
- Gas Phase
  - Spray pyrolysis
  - Inert gas condensation
- Liquid Phase
  - Solvothermal reaction
  - Sol-gel
  - Micellar structured media
- Requirements
  - Simple process
  - Low cost
  - Continuous operation
  - High yield





Spray pyrolysis

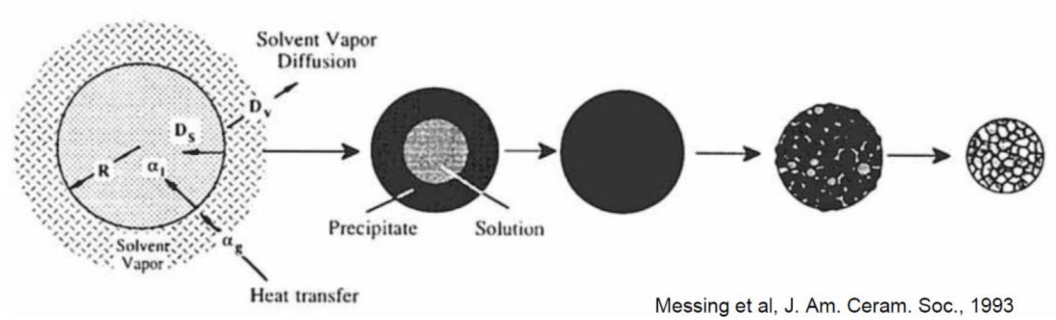
- Starting solution is atomized into small droplets
- Droplets are passed through the furnace where
  - They dry up
  - A reaction is facilitated
- Solid particles are generated when cooling



Spray pyrolysis – Droplet evolution

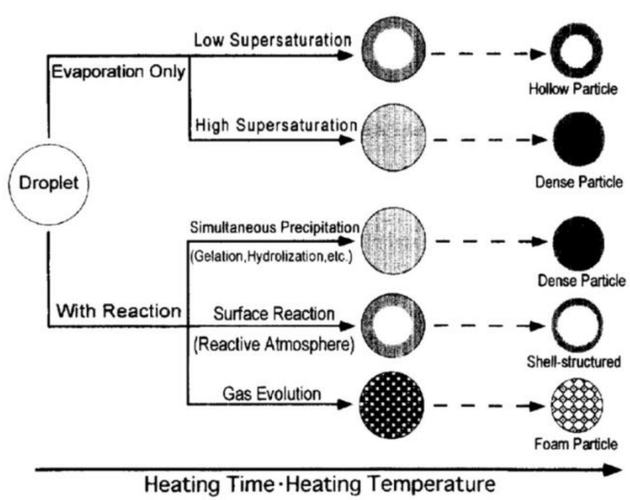
- From droplets, NPs are generated

Evaporation Precipitation Drying Decomposition Sintering

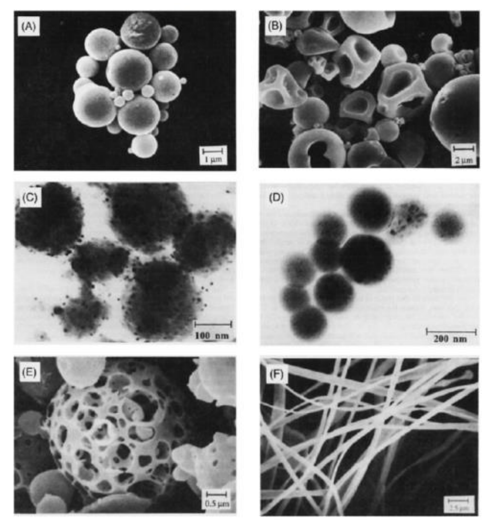


Messing et al, J. Am. Ceram. Soc., 1993

- Precipitation control



Che et al, J. Aer. Sci., 1998



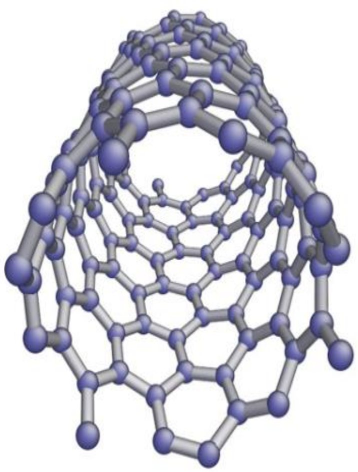
Summary table

	Bottom-Up		
• Gas/Liquid phase • Spray pyrolysis • Solvothermal • Sol-Gel • Efficiency and yield			
NPs	CNTs	NWs	2D

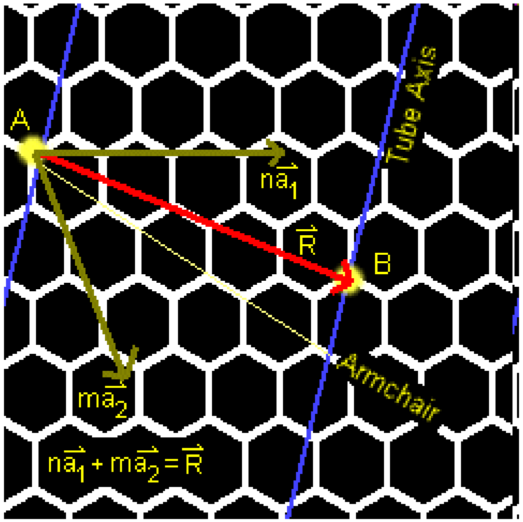
Carbon Nanotubes

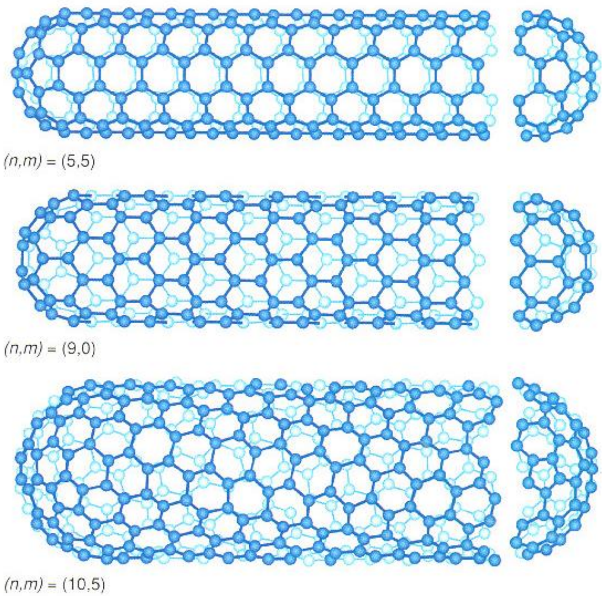
- Arc discharge
- Laser ablation

- CVD
  - Catalytic reaction – requires seed material
  - Potential for upscaling process



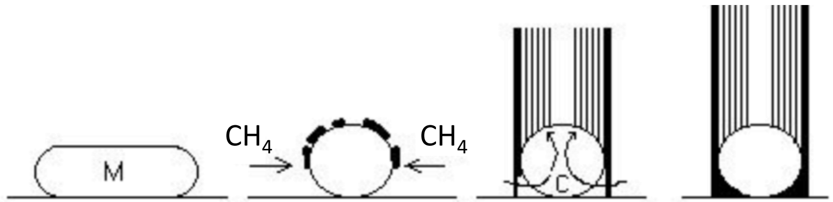
Φ = 0.4 – 2 nm

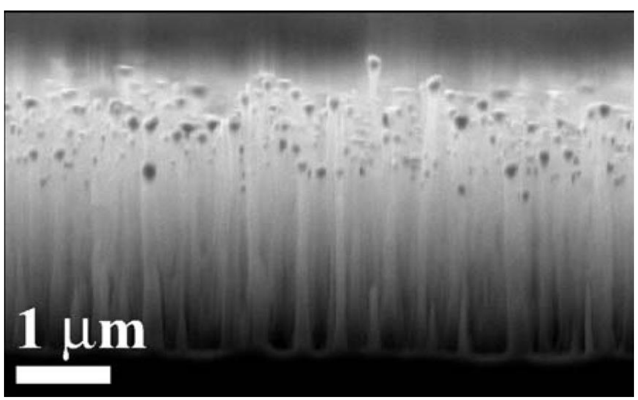


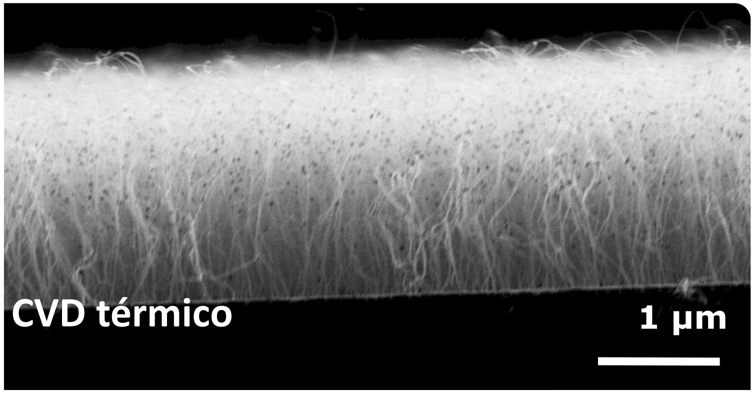


CNTs by CVD

- Metal catalyst particles, e.g. nickel, cobalt, iron…
- Nanotubes grow from those particles
  - Gas reacts at the surface of the catalyst
  - Carbon is transported to the edges of the particle
- This allows for direct grow on the desired substrate



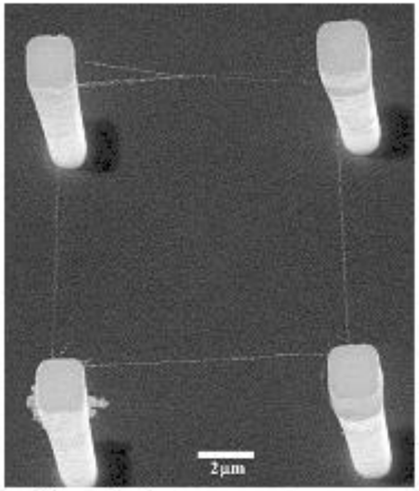




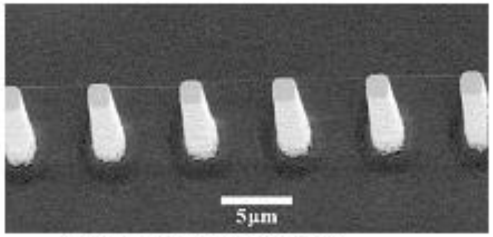
Challenges in CNTs

- Controlling position and direction of growth
  - Catalyst particles
- Controlling chirality
- Reduction of CNT diameter
  - Single wall CNTs are challenging using CVD and catalysts

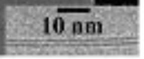
- Remember that it is always needed to use Top-Down methods to enable contact of CNTs to the “Macro-World”



Nanotube square



Nanotube powerline



TEM: Single-Walled

Summary table

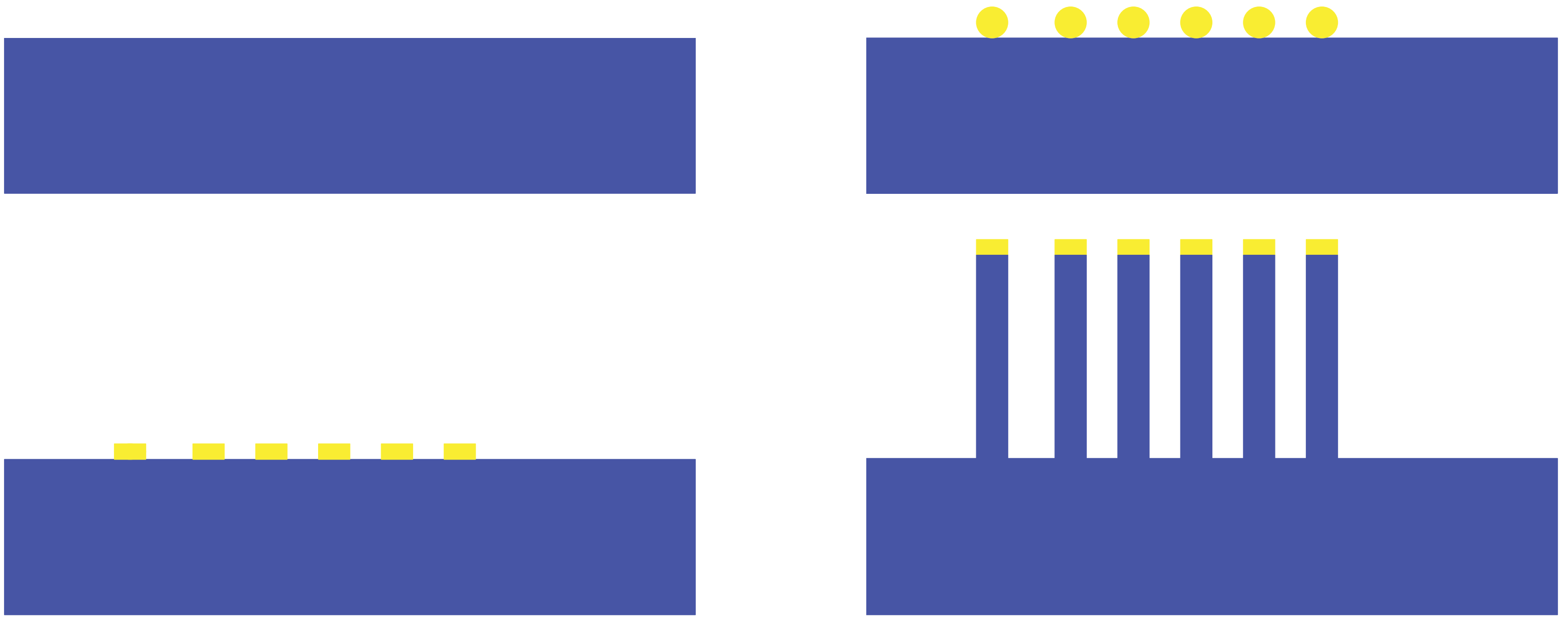
Bottom-Up			
• Gas/Liquid phase • Spray pyrolysis • Solvothermal • Sol-Gel • Efficiency and yield	• Arc-Discharge • Laser ablation • CVD • Position, orientation, size		
NPs	CNTs	NWs	2D

Nanowires

- Solution-phase synthesis
- Vapor-Liquid-Solid growth (VLS)
- MBE, MOCVD, MOVPE

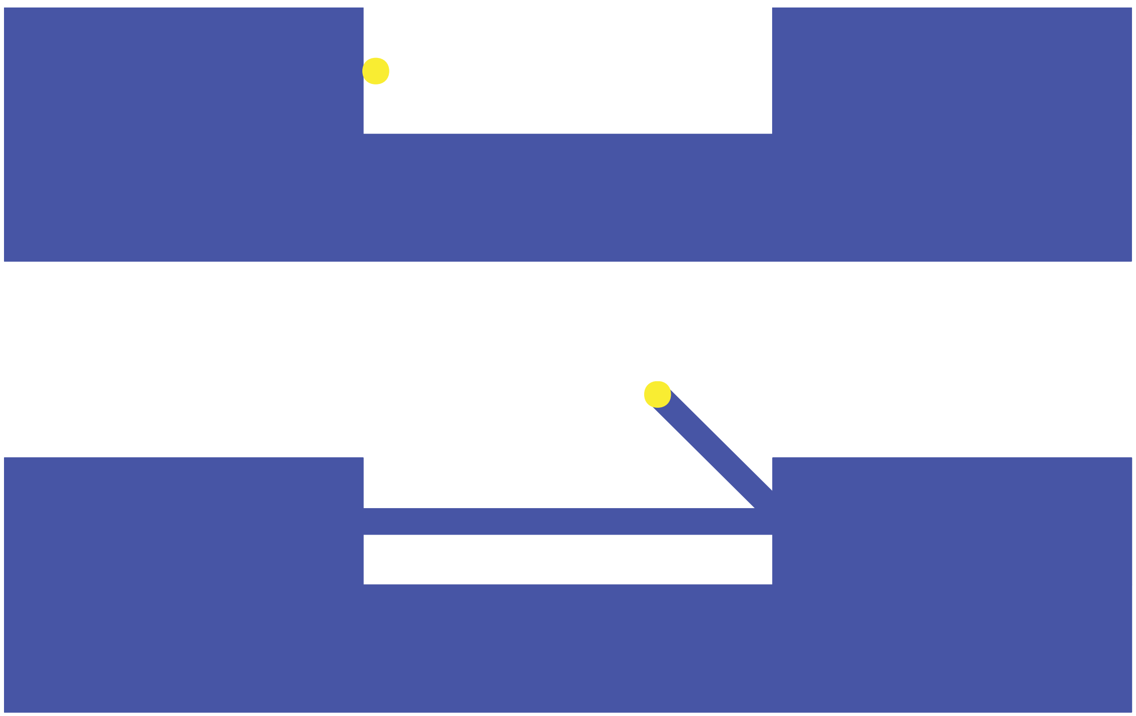
VLS Growth

- Metal catalyst
- SiHx, GeHx, BHx… gas(es) as precursor(s)
- Sidewalls are defined by specific crystallographic planes
  - Almost no roughness



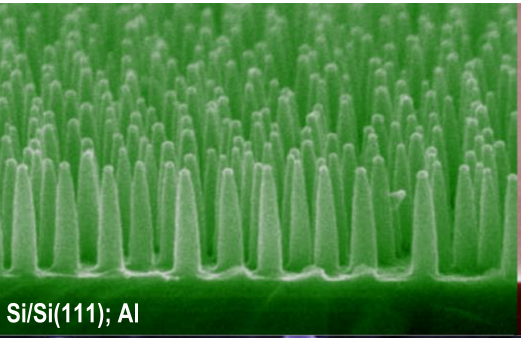
VLS Growth

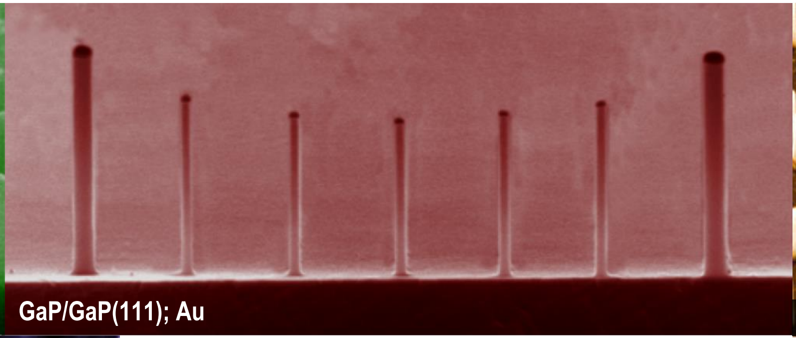
- Metal on sidewalls

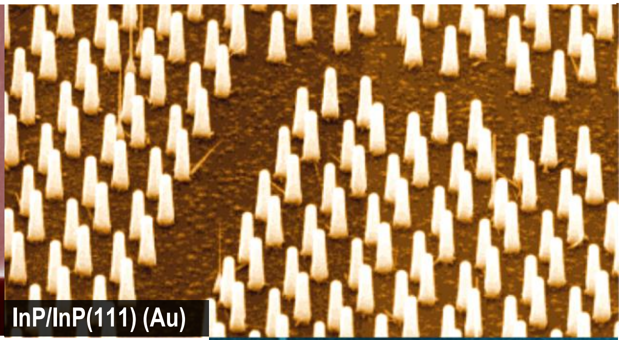


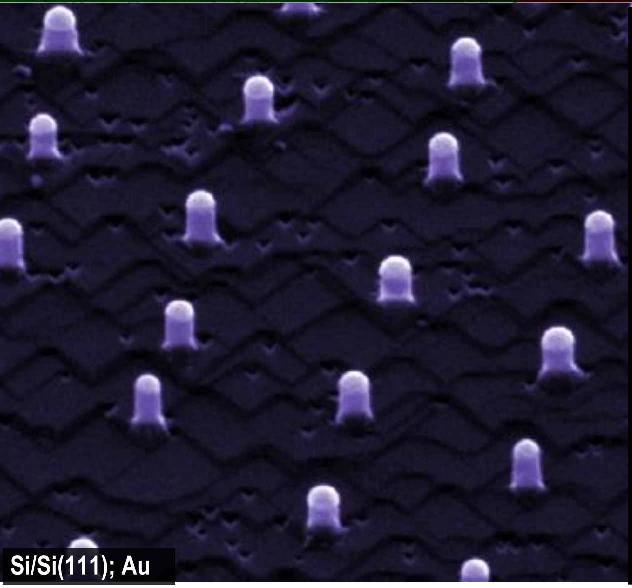
VLS Growth

- Different catalyst…

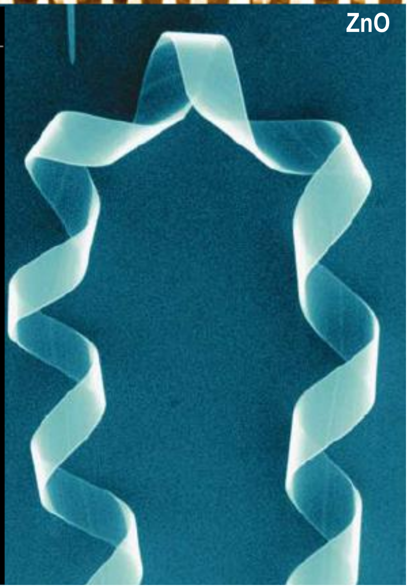






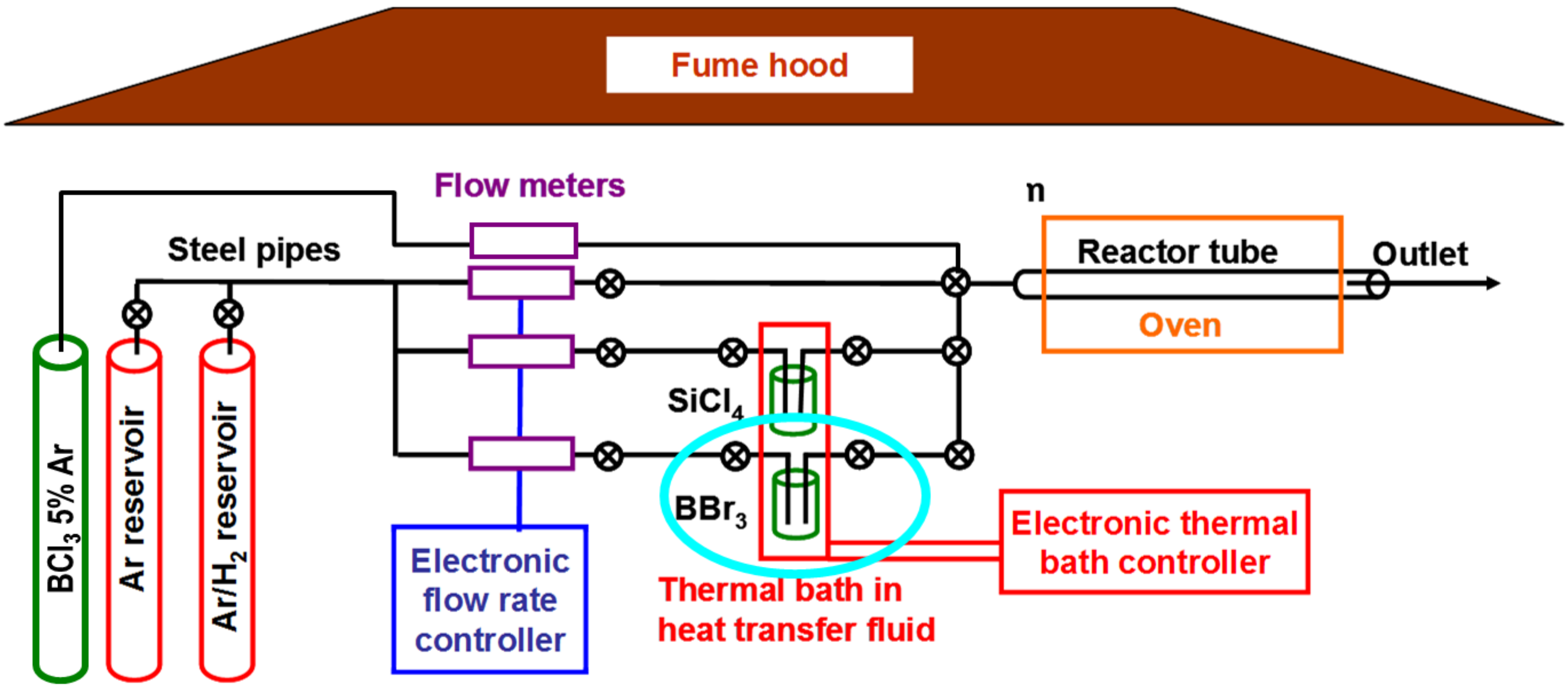


NW material	Source	Metal catalyst	Growth process[a]
Si	$SiCl_4$	Au	CVD
Si	$SiCl_4$	Au, Ag, Cu, Pt	CVD
Si, Ge	SiH_4, GeH_4	Au	CVD
Si	SiH_4	Au	CVD
Si, Ge		Fe, Si/Fe, Ge/Fe	PLD
Si	Si_2H_6	Au	CBE
GaAs	GaAs/Au	Au	PLD
InP	InP/Au	Au	PLD
CdSe	CdSe/Au	Au	PLD
Si	Si	Ga	microwave plasma
GaAs	Et_3Ga, Bu_3As	Au	CBE
ZnO	ZnO, C	Au	evaporation
Si	Si	Au	MBE
Si	SiO	Au	evaporation
Si	silyl radicals	Ga	microwave plasma etching
Si	SiH_4 or SiH_2Cl_2	Ti	CVD
GaAs/GaP	GaAs/GaP	Au	PLD
GaAs/InAs	Me_3Ga, Bu_3As, Me_3In	Au	CBE
Si/SiGe	$SiCl_4$	Au	Si: CVD; Ge: PLD



VLS Growth

- Doping Si NWs



Challenges

- Contacting the NWs with the “macro” world
  - Usually Top-Down techniques are required

Bottom-up assembly of large-area nanowire resonator arrays

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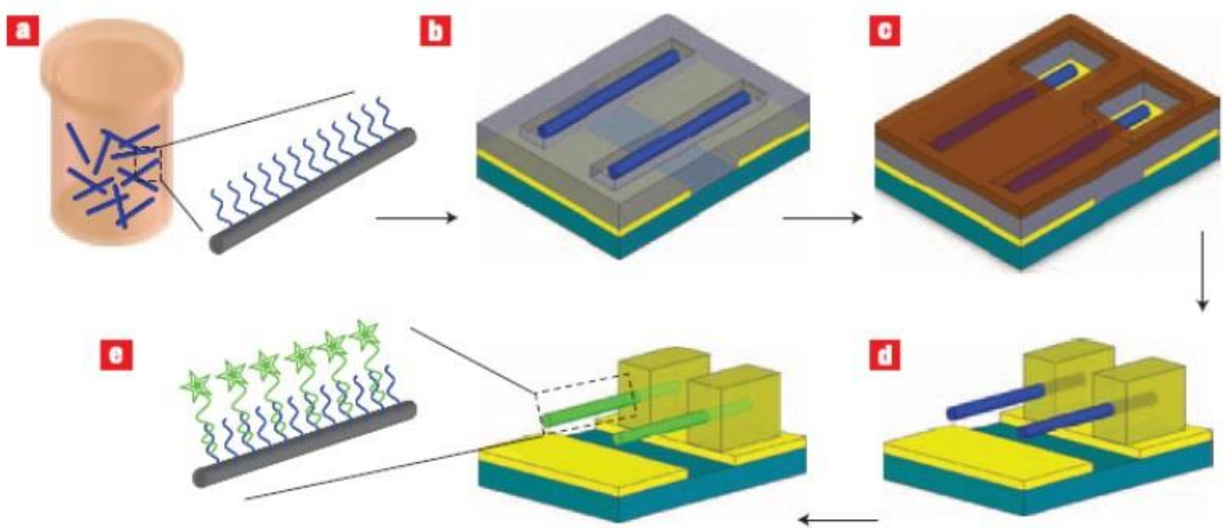
  - Interesting example:
    - Long-range dielectrophoretic forces attract nanowires to surface and align them along the field gradient
    - Short-range capacitive forces further centre the NWs in the wells



Summary table

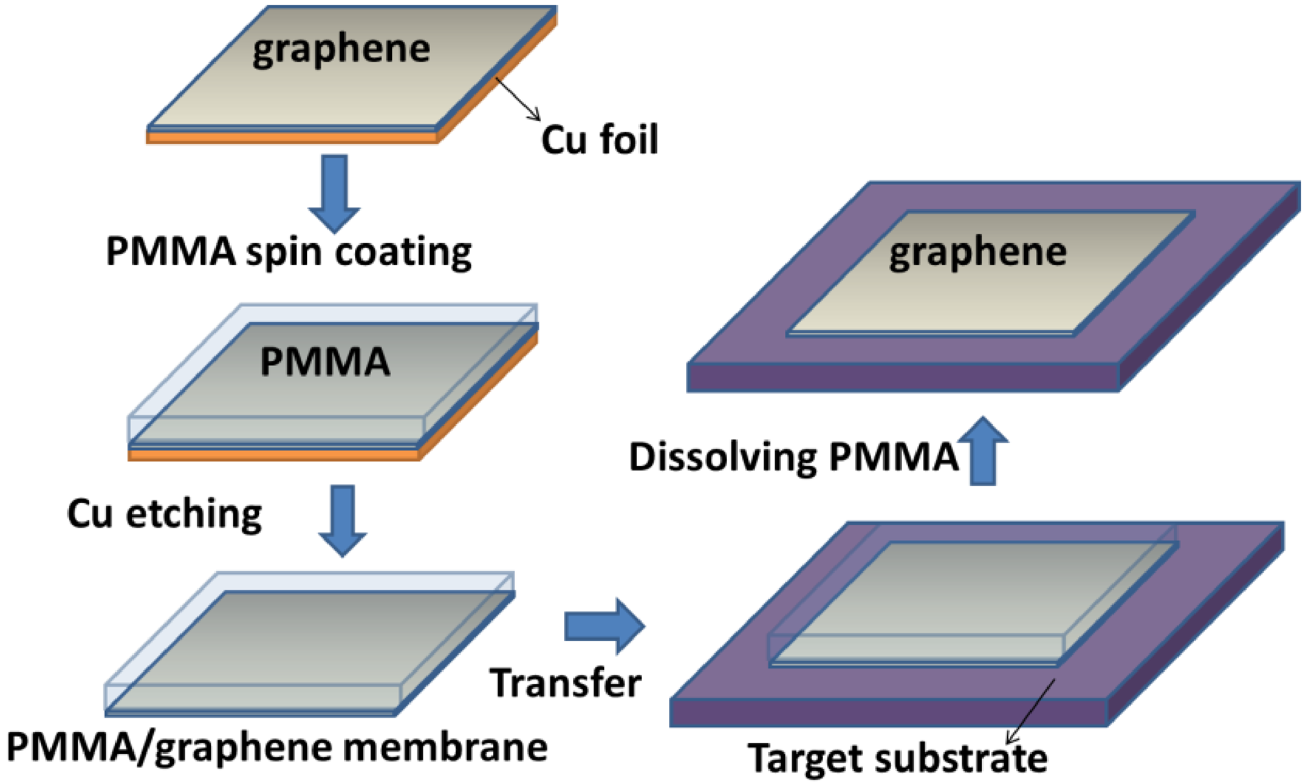
Bottom-Up			
NPs	CNTs	NWs	2D
• Gas/Liquid phase • Spray pyrolysis • Solvothermal • Sol-Gel • Efficiency and yield	• Arc-Discharge • Laser ablation • CVD • Position, orientation, size	• VLS Growth • MBE • Well defined sidewalls • Position, size	

Graphene

- CVD
  - Catalyzed reaction on Ni, Cu
  - More layers depending on diffusion coefficient of C in the metal
- Exfoliation

Graphene transfer

- CVD on a substrate and then transferred to a different substrate



Summary table

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• Gas/Liquid phase • Spray pyrolysis • Solvothermal • Sol-Gel • Efficiency and yield	• Arc-Discharge • Laser ablation • CVD • Position, orientation, size	• VLS Growth • MBE • Well defined sidewalls • Position, size	• CVD on SiC, Cu, Ni… • Exfoliation with scotch tape

Take home message

- From micro to nano
- Easy connection to "macro"
- Very high cost to reduce dimensions

TOP-DOWN

Deposition
- Wet&Dry oxidation of Si
- Chemical processes
- Physical processes
- Lift-off – pattern without etching

Implantation
- Dope Si – transistors, etc.
- Generate new substrates – SOI
- Ion energy and dose
- Annealing is critical for "nano"

Etching
- Wet etching – Purely chemical
- Dry etching – can be tuned between chemical and physical
- Issues – uniformity, reproducibility

Lithography
- Method to "draw" on the wafer
- Optical, EBL, NIL, …
- Best option depends on design, requirements and $$$

- Direct growth/synthesis of structures
- Very cheap & high quality
- Difficult connection to "macro"

Bottom-Up

NPs
- Gas/Liquid phase
- Spray pyrolysis
- Solvothermal
- Sol-Gel
- Efficiency and yield

CNTs
- Arc-Discharge
- Laser ablation
- CVD
- Position, orientation, size

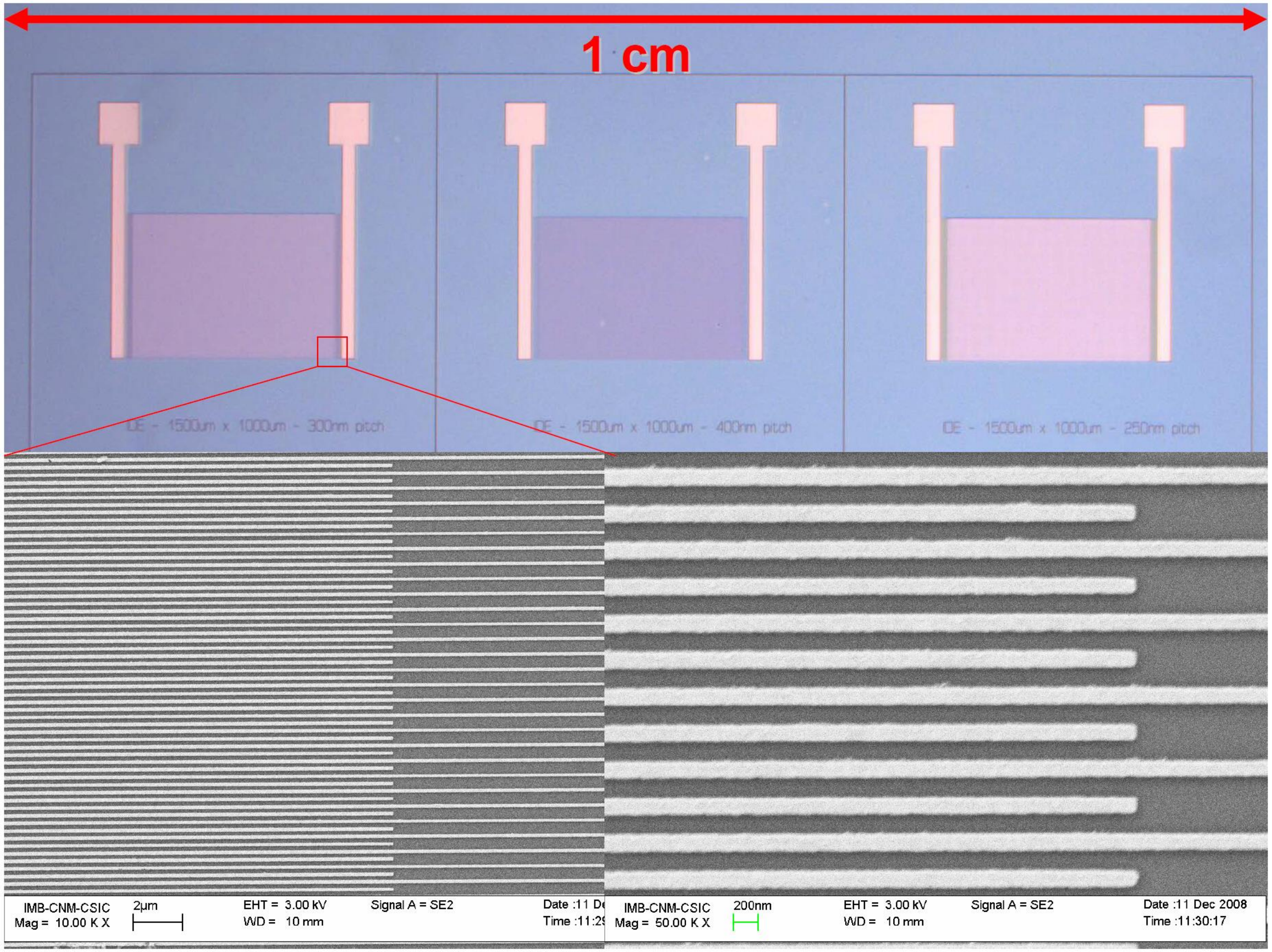
NWs
- VLS Growth
- MBE
- Well defined sidewalls
- Position, size

2D
- CVD on SiC, Cu, Ni…
- Exfoliation with scotch tape

Exercises

Gold Interdigitated Electrodes

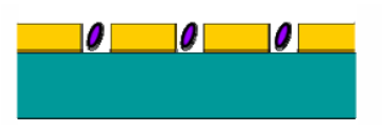
- Two distinct parts: electrodes (nano-size) and metal leads (micro/milli)

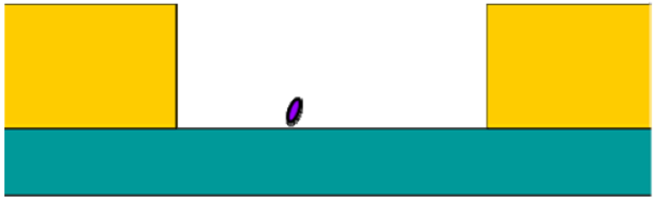


Gold Interdigitated Electrodes

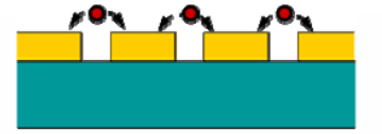
- Two distinct parts: electrodes (nano-size) and metal leads (micro/milli)

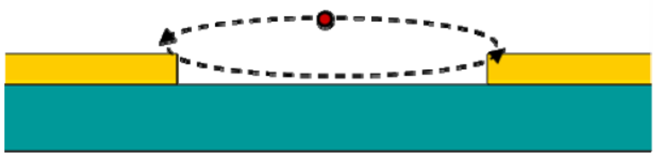
- Improved sensitivity when compared to larger electrodes





- Faster response time





Gold Interdigitated Electrodes
How would you proceed for their fabrication?

A. Option #1
B. Option #2
C. Option #3
D. Option #4

Option #1
- Optical litho
- PVD sputtering
- Wet chemical etching

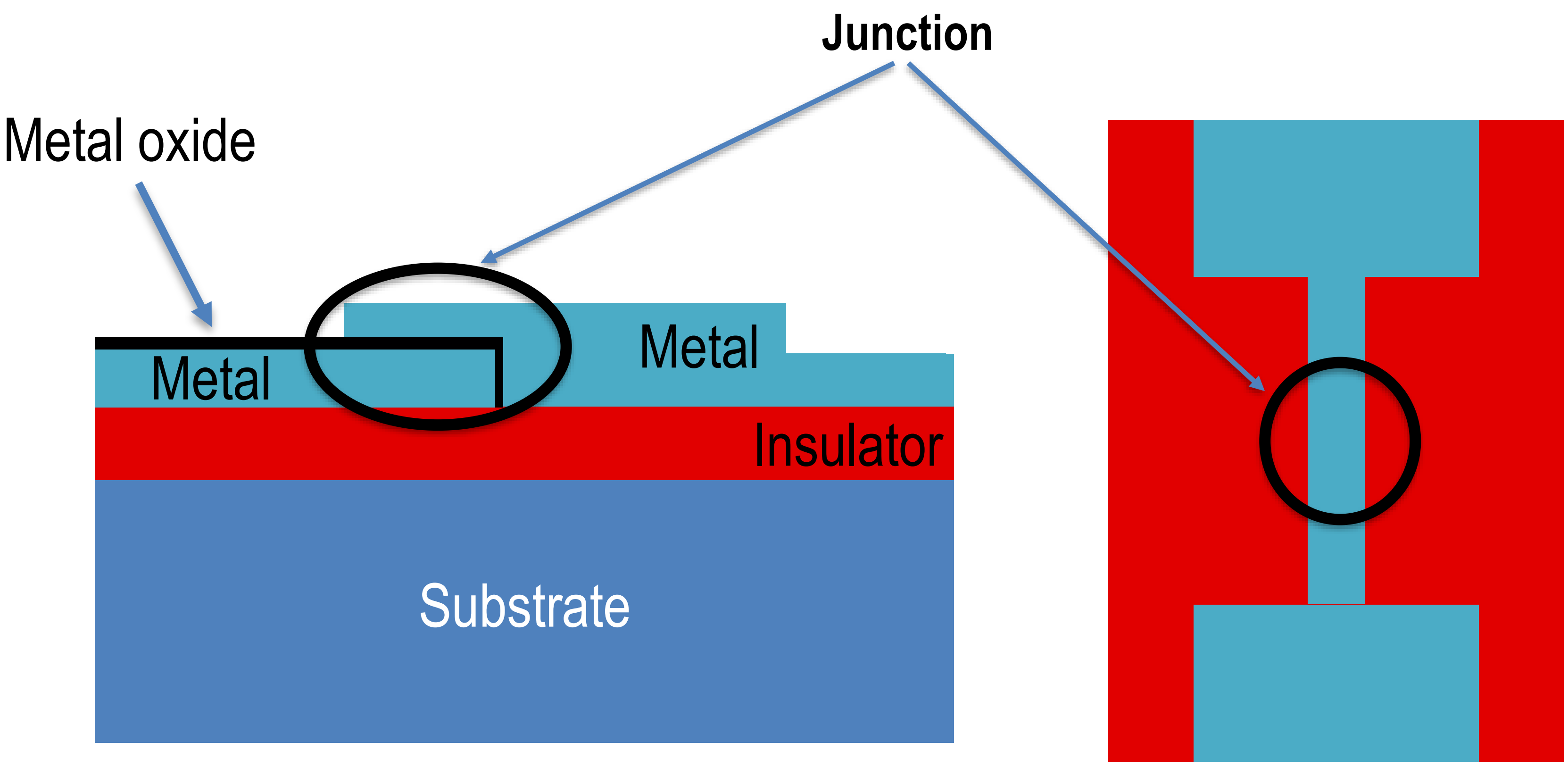
Option #2
- EBL
- PVD evaporation
- Dry etching

Option #3
- Two levels
- CVD of metal
- EBL
- Lift-off

Option #4
- Two levels
- PVD evaporation
- EBL+Optical litho
- Dry etching

Tunnel junctions – Josephson Junction

- Two metals separated by an oxide
- Oxide is less than 3 nm thick
- Lateral dimensions in the order of 100 nm



How would you fabrication such a tunnel junction?

A. Option #1
B. Option #2
C. Option #3
D. Option #4

A	B	C	D	0

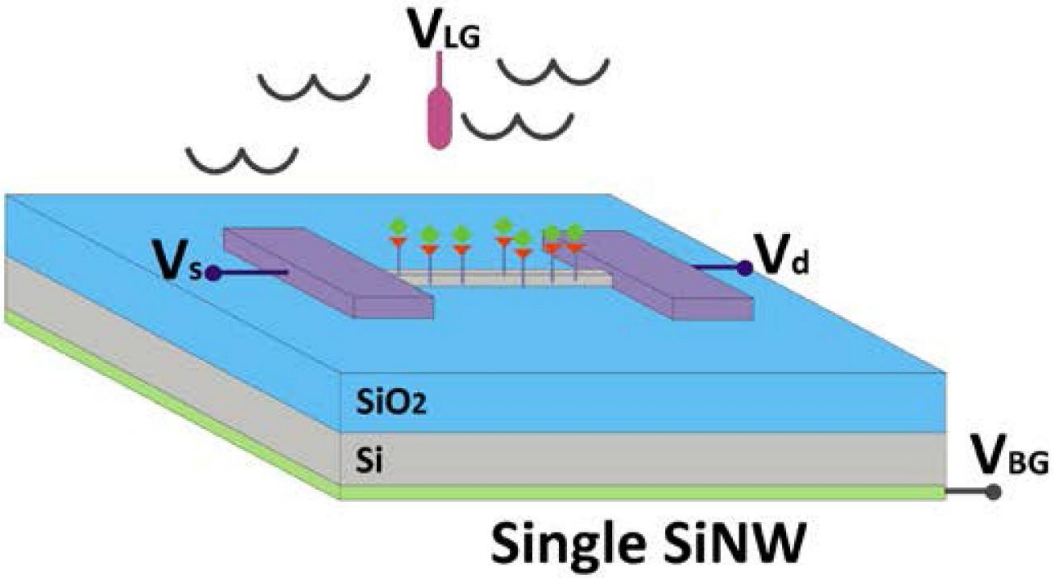
Option #1
- EBL
- 2 lithographies
- 2 Metallizations
- 2 Lift-offs

Option #2
- EBL
- 2 lithographies
- 2 Metallizations
- 2 Dry etchings

Option #3
- EBL
- Evaporation
- Lift-off

Option #4
- Optical litho
- Sputtering
- Dry etching

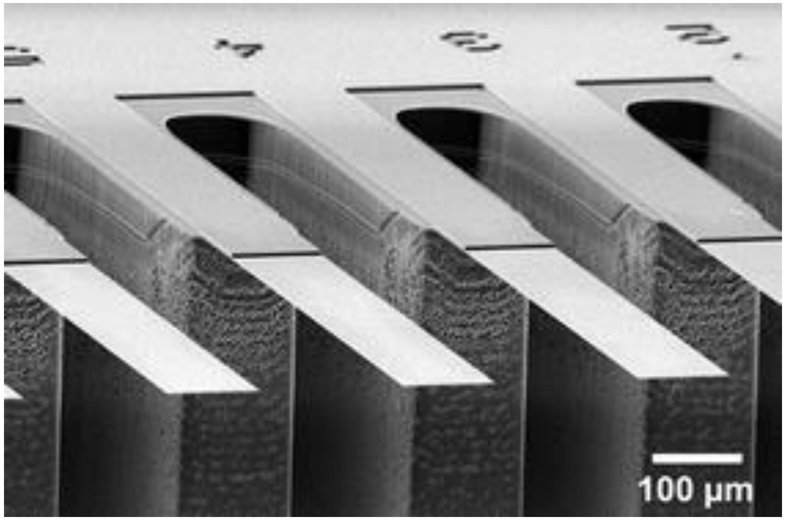
SiNW FET



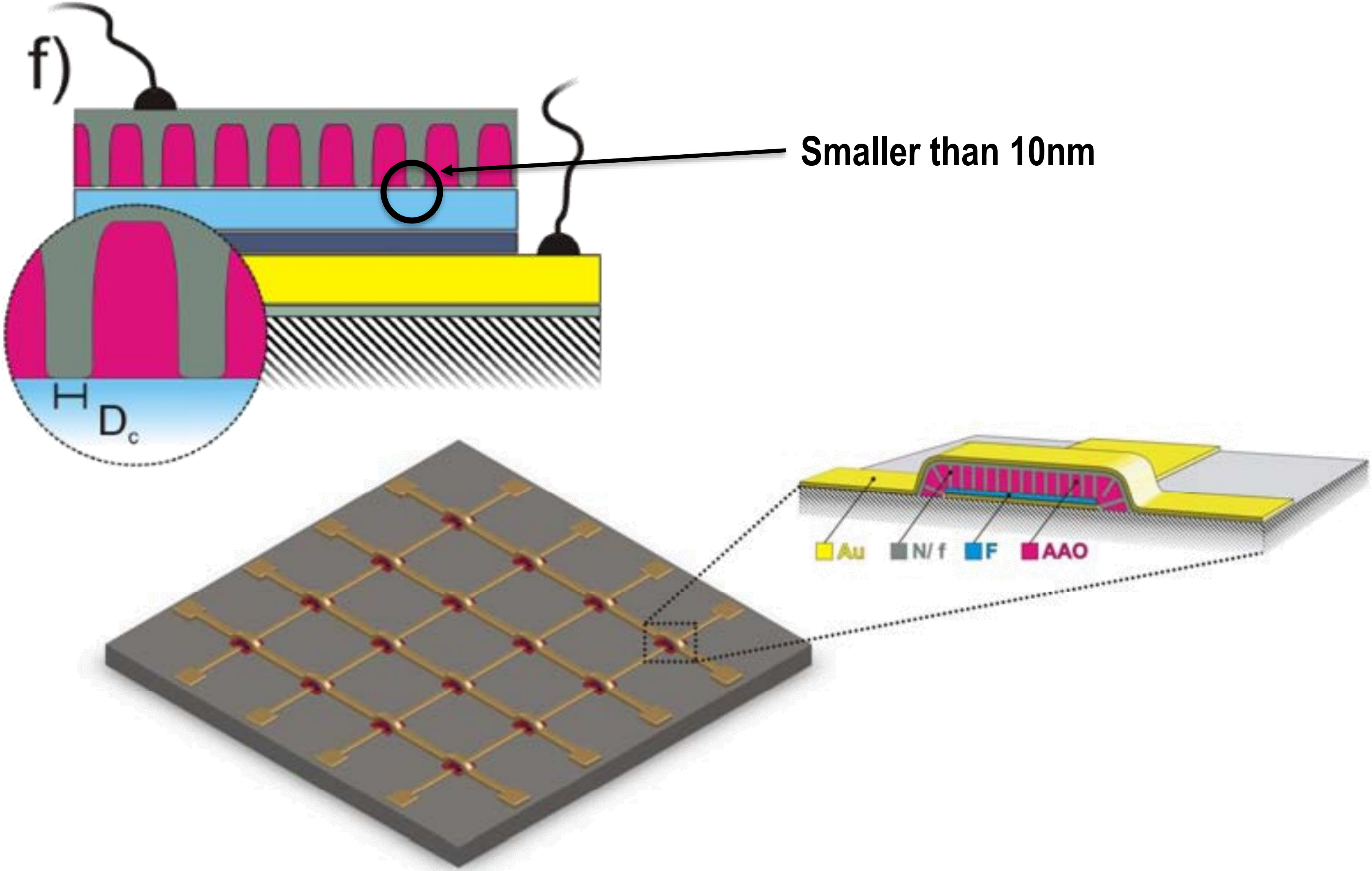
How would you fabricate a SiNW FET?

A. Bottom-up synthesis
B. Top-Down Dry etching
C. Top-Down wet etching
D. Post-definition oxidation

Silicon mechanical cantilevers



Quantum Point Contacts (Julian)



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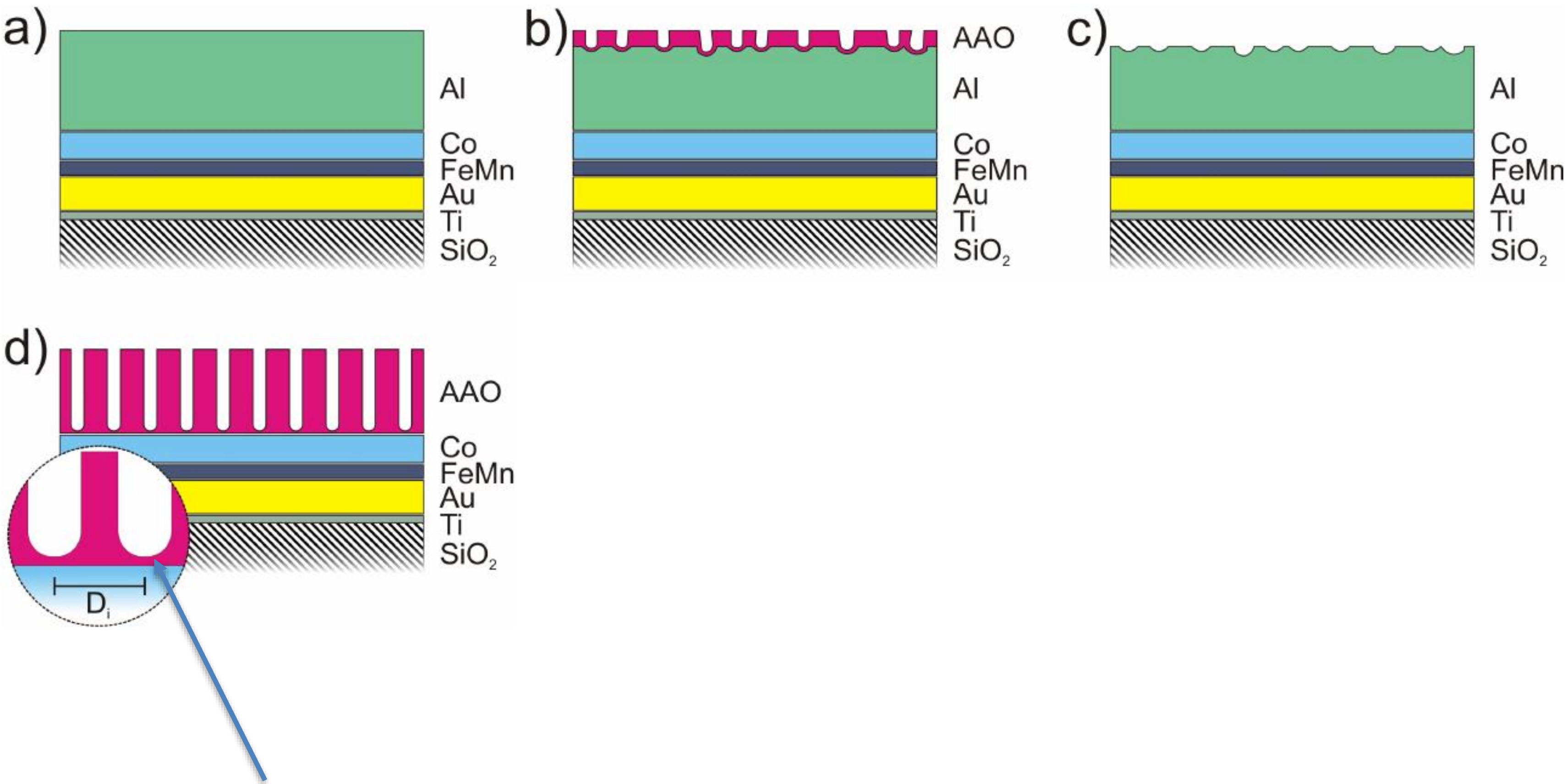

Residual layer of insulator

What would you use to etch that residual layer?

A. Chemical Dry etching
B. Physical Dry etching
C. Wet etching

http://lgv.participoll.com/